Enabling Visual Communication

LEADIS®

LDS176

Data Sheet

396 Segment (132 x 3) + 132 Common
4,096 Color One-Chip MLA Driver

Feb. 15, 2005 PRELIMINARY

CONTENTS

Document No: LTT176DS-010

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REVISION HISTORY

Date	Contents	Version
May 22, 2004	- Preliminary Version 0.0	Ver 0.00 (Preliminary)
Feb. 15, 2005	- Final Version 0.1 - Page 2, 4 and 157: ROWM pad changed to TEST6 - Page 3 and 156: TESTF pad changed to TESTF1 to TESTF26 - Page 3 and 157: ID2/ID1/ID0 pads changed to TEST7 SRGB/SMX/SMY pads changed to TEST8 - Page 151: Section 8.2 updated	Ver 0.10 (Final Version)

1 DESCRIPTION

LDS176 is a single chip low power CMOS LCD controller/driver for color STN displays of 132 rows and 132xRGB columns. It has a 209k-bit (132 x 12bit x 132) display RAM and a full set of control functions. LDS176 uses the Multiple Line Addressing technique in order to achieve better optical performance with lower power consumption. LDS176 offers 3 microprocessor interfaces: 8080-system, 6800-system and 3-line serial interface.

2 FEATURES

Single chip LCD controller/driver

132 row and 396 (132 x RGB) column outputs

Low cross talk by mixed control (FRC + PWM)

Display mode

Color modes:
- Full colors (Idle mode off): 4096-color (16-gray scale)
- Reduced color (Idle mode on): 8-colors (3-bit binary mode)

Interface modes:

Color modes on the display host interface:
- 8 bit/pixel: (RGB) = (332) using the 209k-bit frame memory and a look up table (LUT)
- 12 bit/pixel: (RGB) = (444) using the 209k-bit frame memory directly
- 16 bit/pixel: (RGB) = (565) using the 209k-bit frame memory with dithering (16 bit/pixel to 12 bit/pixel)

Display data RAM (frame memory): 132 x 132 x 12-bit = 209k bit

Interfaces:

3-line serial interface
8-bit interface with 8080-series MPU
8-bit interface with 6800-series MPU

Display features

Area scrolling
Partial display mode
Software programmable color depth mode
N-line inversion for low cross talk

On chip:

Oscillator for display system requires no external components (external clock also possible)
Generation of VLCD
Temperature compensation of VLCD

Logic supply voltage range VDD1 to VSS

1.65 to 1.95V

Analog supply voltage range for VLCD generation VDD2 to VSS2:

2.6 to 2.9V

Display supply voltage range (VLCD=VH-VL)

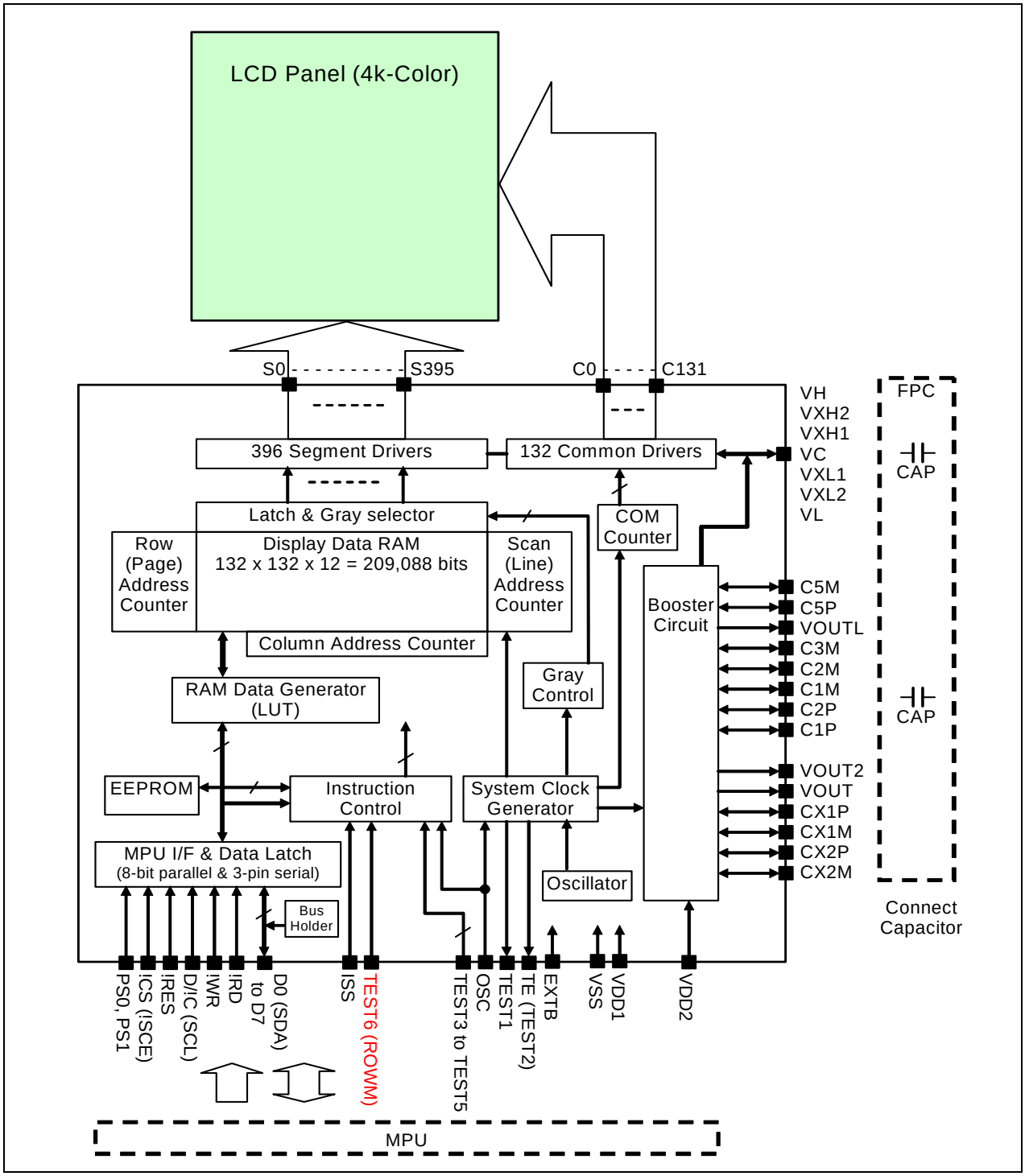
Max 18V

Low power consumption, suitable for battery operated systems

CMOS compatible inputs

Optimized layout for COG assembly

3 BLOCK DIAGRAM



4 PIN DESCRIPTION

Table 4.1.1 Pin Description

Name	Type	Description
LCD row and column pins		
S0 to S395	O	LCD segment (column) driver outputs
C0 to C131	O	LCD common (row) driver outputs
Power supply pins		
VDD1	P	Power supply for I/O system
VDD2	P	Power supply for logic, analog system and boosting input voltage
VSS	P	System ground for internal system
VSS1	P	System ground for a manufacturer's special use. Should be connected to VSS.
LCD supply pins		
*1) VH	I/O	LCD common driver bias level
*1) VXH2	I/O	LCD segment driver bias level
*1) VXH1	I/O	LCD segment driver bias level
*1) VC	I/O	LCD segment/common driver bias level
*1) VXL1	I/O	LCD segment driver bias level
*1) VXL2	I/O	LCD segment driver bias level (Connect to VSS pad)
*1) VL	I/O	LCD common driver bias level
LCD supply voltage generation		
CX1P, CX2P CX1M, CX2M	I/O	Capacitor connection pin for booster1 circuit.
VOUT	O	Output of booster1 circuit (output of 3-times booster). Connect capacitor to VSS (GND)
VOUT2	O	Output of booster1 circuit (output of 2-times booster). Connect capacitor to VSS (GND)
C1P, C2P C1M to C3M	I/O	Capacitor connection pin for booster2 circuit.
VOUTL	O	Output of booster2 circuit. Connect capacitor to VSS (GND)
C5M	I/O	Capacitor connection pin for booster3 circuit.
C5P	I/O	Capacitor connection pin for booster3 circuit.
Clock input and ID pins		
OSC	I	Oscillator input for test purpose.
Test pins		
TEST1	O	Test pin, not accessible to user must be left open.
TEST3, TEST4, TEST5	I	Test input pins, should be connected to VDD1 or VSS.
TESTF1 to TESTF26	I	Test input pins, should be left open.
TEST7, TEST8	I	Test input pins, should be connected to VDD1 or VSS.

Table 4.1.2 Pin Description (continued)

Name	Type	Description
Host interface pins		
ISS	I	Instruction set selection (“0”: code set0, “1”: code set1).
PS0, PS1	I	Interface mode setting (Refer Section 5.1 MPU INTERFACE)
!RES	I	External reset This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
!CS (!SCE)	I	Chip select input pin (“Low” enable). This pin can be permanently fixed “Low” in parallel interface mode only. If !CS is connected to ground in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.
D/!C (SCL)	I	Display data / Command selection pin in parallel interface. In serial interface, this pin used as serial clock (SCL).
!WR (R/!W)	I	Write enable in 8080-series parallel interface. Read write selection in 6800-series parallel interface. In serial interface, connect this to VDD1 or VSS.
!RD (E)	I	Read enable in 8080-series parallel interface. Read/write enable in 6800-series parallel interface. In serial interface, connect this to VDD1 or VSS.
TE	O	Tearing effect output.
D7 to D0(SDA)	I/O	8-Bit bi-directional display data / command bus for 8-bit parallel interface. In serial interface, D0 is used as serial data input/output (SDA). In serial interface, unused pins (D7 to D1) can be open or connect to VDD1 or VSS.
Mode Select		
EXTB	I	Extended command code access pin. To use extended command set (like EEPROM program), please connect this to VSS. During normal operation, please open this pin.
TEST6	I	TEST input pin Please connect this to VSS.

NOTE: DUMMY – These pins should be open (float).

**1) Voltages should have the following relationship: VH ≥ VXH2 ≥ VXH1 ≥ VC ≥ VXL1 ≥ VXL2 (VSS) ≥ VL ≥ VOUTL*

2) When in serial mode (PS0 = Low) then if some data or signal appears on !WR, !RD and D7 to D1 then it will have no influence to the system. Also in Parallel mode (PS0 =High) there will be no influence to the serial interface.

3) When !CS is high, there is no influence to the serial or parallel interfaces.

4) If !CS is connected to ground in Parallel Interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore, there will be no influence to the Power Consumption of the Display Module.

5 FUNCTIONAL DESCRIPTION

5.1 MPU INTERFACE

LDS176 can interface with MPU at high speed. However, if the interface cycle time is faster than the limit, MPU needs to have dummy wait(s) to meet the cycle time limit.

5.1.1 Interface Type Selection

The selection of a given interfaces are done by setting PS0, PS1 and PS2 pins as shown in ***Table 5.1.1***.

Table 5.1.1 Interface Type Selection

PS0	PS1	Interface	Read back select
0	-	3-Line Serial	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
1	0	6800 MPU 8-bit Parallel	E strobe (8-bit read data and 8-bit read parameter)
1	1	8080 MPU 8-bit Parallel	!RD strobe (8-bit read data and 8-bit read parameter)

5.1.2 General Protocol

For programming of the LCD driver, the general supported protocol is shown in ***Fig. 5.1.1***

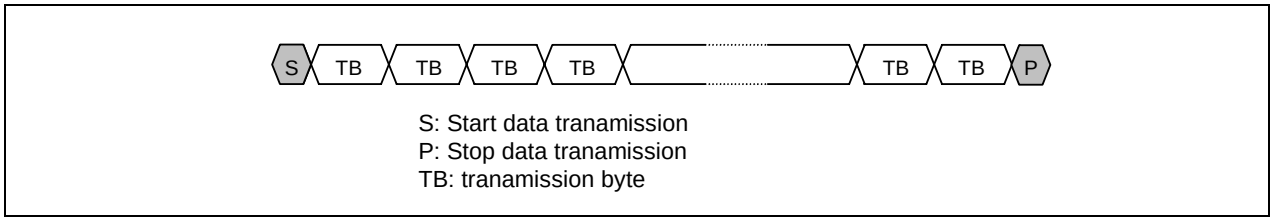


Fig. 5.1.1 Programming protocol

If data write or parameter write is interrupted by any other command, data write command or parameter write command should be done again to write the remained data or parameter.

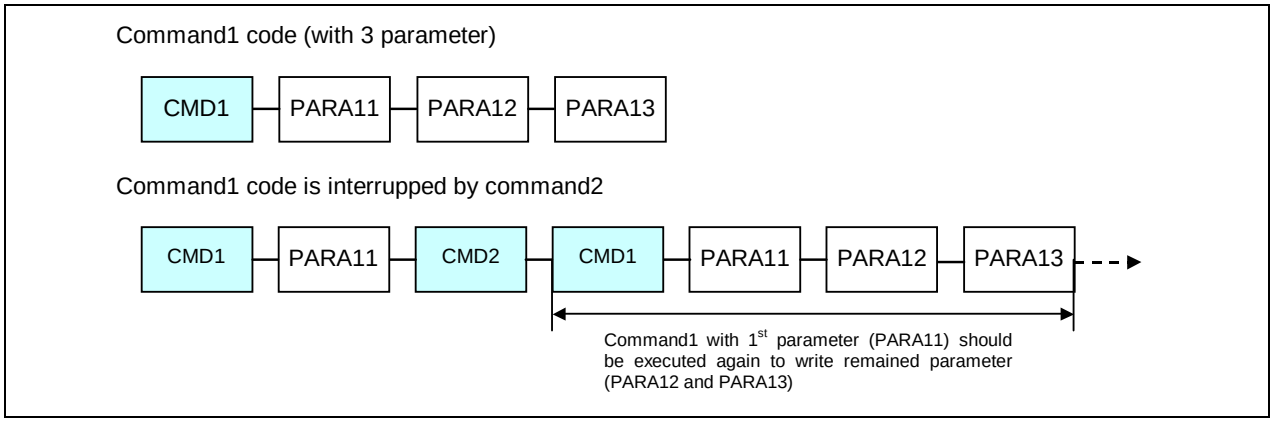


Fig. 5.1.2 Write interrupt sequence

5.1.3 8080-Series Parallel Interface (PS0 = "High", PS1="High")

The 8080-series bi-directional interface can be used for communication between the micro controller and the LCD driver chip. The selection of this interface is done with PS0 and PS1 pin.

The interface functions of the parallel interface (8080-series) are given in ***Table 5.1.2.***

Table 5.1.2 Parallel Interface Function

D/!C	8080-series		Function
	!RD	!WR	
1	1	↑	Write 8-bit display data or 8-bit parameter (D7 to D0)
0	1	↑	Write 8-bit command (D7 to D0)
1	↑	1	Read 8-bit display data (D7 to D0)
1	↑	1	*1) Read 8-bit parameter or status (D7 to D0)

NOTE: "↑"= rising edge

**1) Applied for command code0 : DAh, DBh, DCh, 04h and 09h*

command code1: DAh, DBh and DCh

The parallel interface timing diagram is given in ***Fig. 5.1.3*** and ***Fig. 5.1.4.***

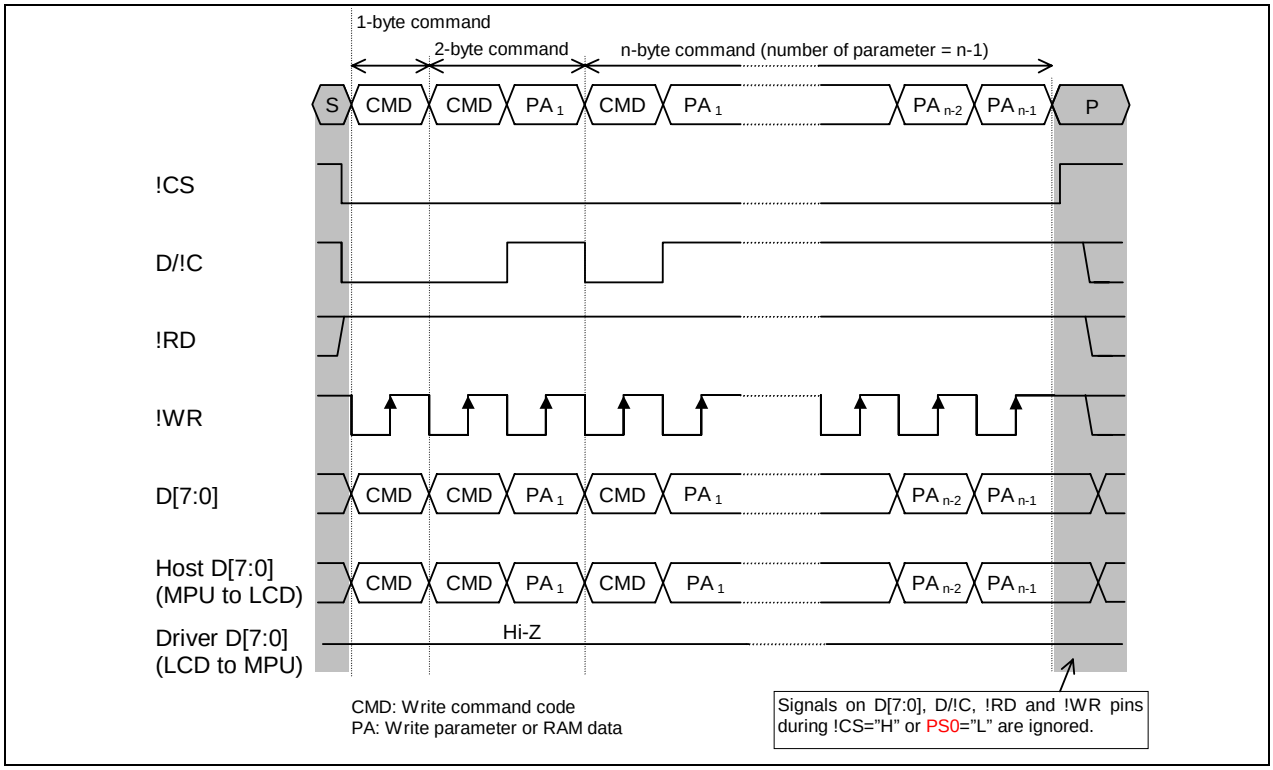
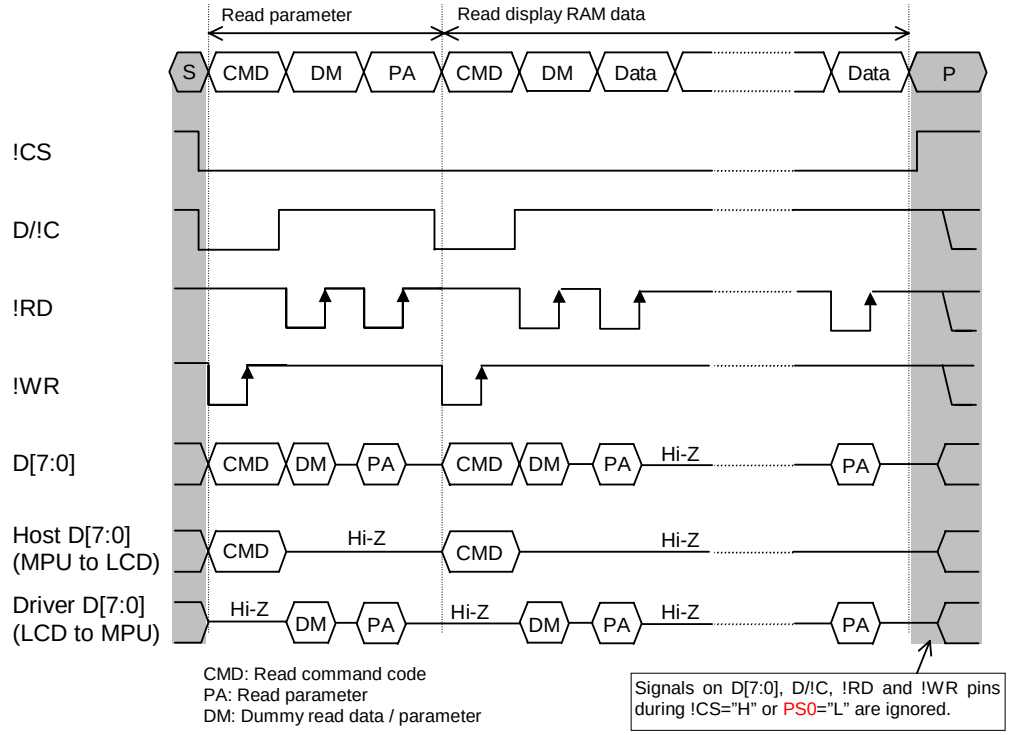


Fig. 5.1.3 8080-Series parallel bus protocol, write to register or display RAM



NOTE: If both D/!C and !RD is "Low", there is no damage on the driver and there is no visible effect on the display, It will be considered as NOP (No operation).

Fig. 5.1.4 8080-Series parallel bus protocol, read from register

5.1.4 6800-Series Parallel Interface (PS0 = "Low", PS1="Low")

The 6800-series bi-directional interface can be used for communication between the micro controller and the LCD driver chip. The selection of this interface is done with PS0 and PS1 pin.

The interface functions of the parallel interface (6800-series) are given in ***Table 5.1.3.***

Table 5.1.3 Parallel Interface Function

D/!C	6800-series		Function
	R/!W	E	
1	0	↓	Write 8-bit display data or 8-bit parameter (D7 to D0)
0	0	↓	Write 8-bit command (D7 to D0)
1	1	↓	Read 8-bit display data (D7 to D0)
1	1	↓	*1) Read 8-bit parameter or status (D7 to D0)

NOTE: "↓"= falling edge

**1) Applied for command code0 : DAh, DBh, DCh, 04h and 09h*
command code1: DAh, DBh and DCh

The parallel interface timing diagram is given in ***Fig. 5.1.5*** and ***Fig. 5.1.6.***

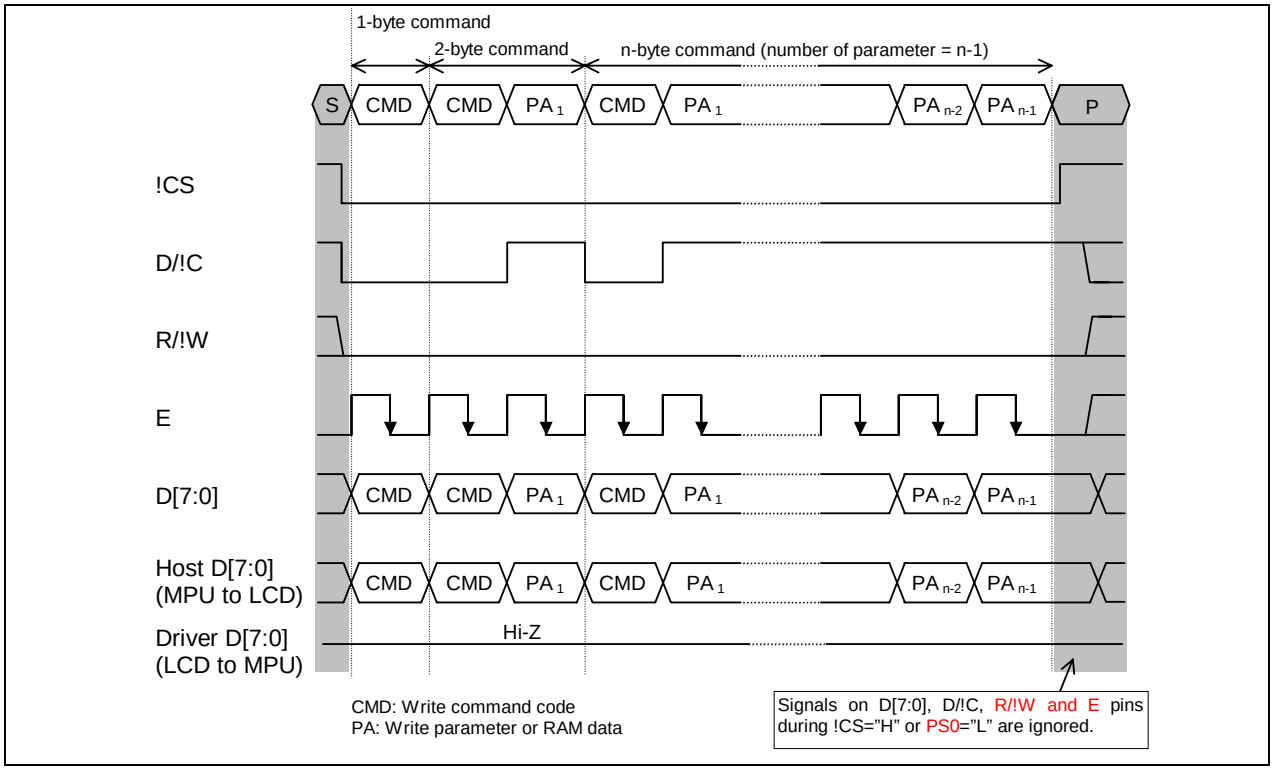


Fig. 5.1.5 6800-Series parallel bus protocol, write to register or display RAM

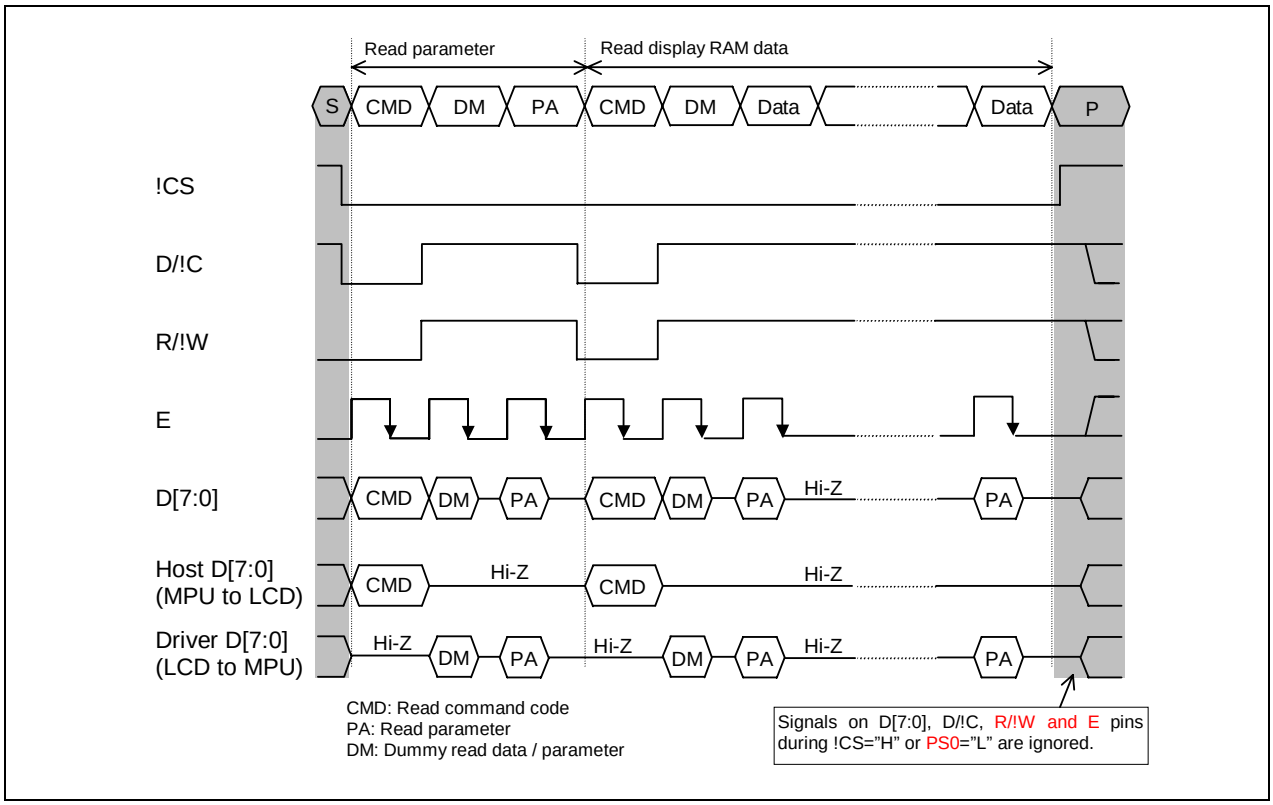


Fig. 5.1.6 6800-Series parallel bus protocol, read from register

5.1.5 Serial Interface (PS0= "Low")

Communication with the microprocessor can also be done via a clock-synchronized serial peripheral interface. The selection of this interface is done with PS0 pin.

The serial interface is a 3-line bi-directional interface for communication between the micro controller and the LCD driver chip. The 3-lines serial use: !SCE (chip enable), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary.

5.1.5.1 Write Mode

The write mode of the interface means the micro controller writes commands and data to the LDS176. 3-Line serial data packet contains a control bit D/!C and a transmission byte. If D/!C is low, the transmission byte is interpreted as command byte. If D/!C is high, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to the LDS176. The MSB is transmitted first. The serial interface is initialized when !SCE is high. In this state, SCL clock pulse and SDA data have no effect. A falling edge on !SCE enables the serial interface and indicates the start of data transmission.

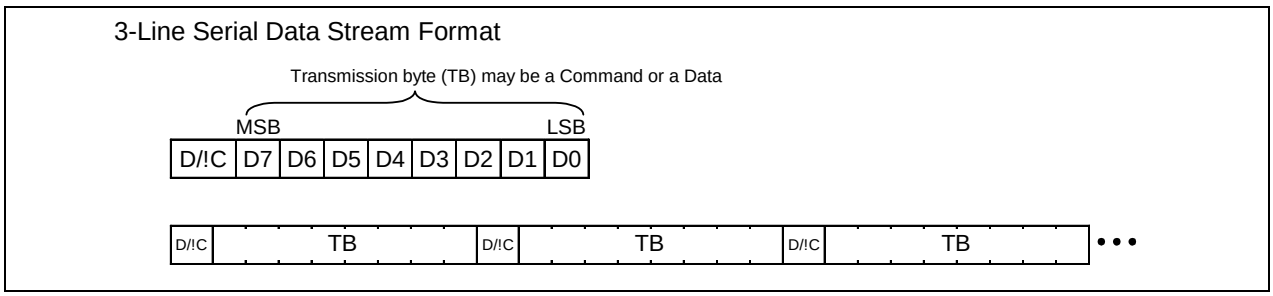


Fig. 5.1.7 Serial data stream, write mode

It is possible to invoke a pause by !SCE while transferring display data or multiple parameter data. If !SCE is high after a whole byte of display data or multiple parameter data has been completed, then LDS176 will wait and continue the display data or multiple parameter data transmission from the point where it was paused as shown in ***Fig. 5.1.8.***

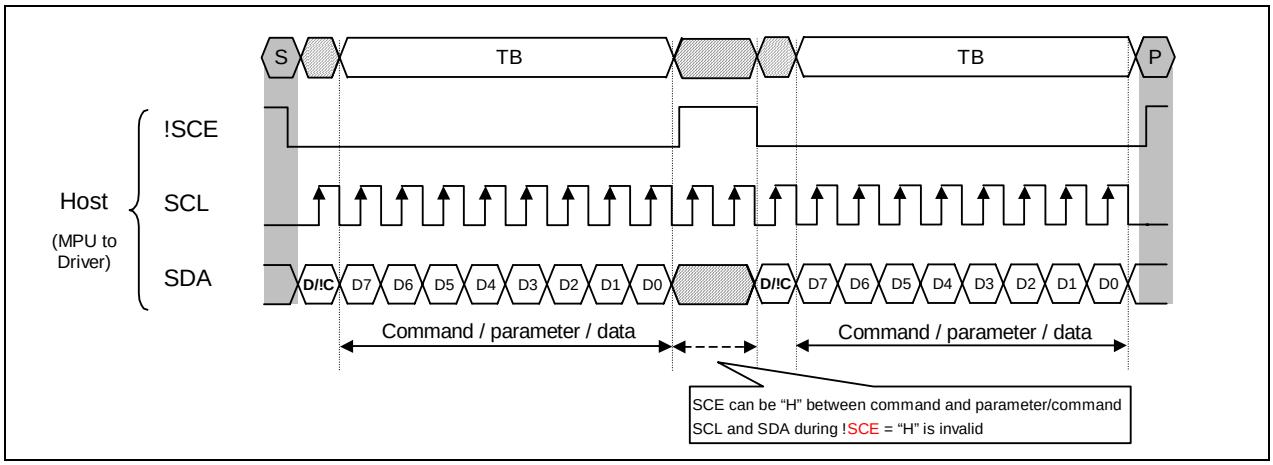


Fig. 5.1.8 Serial bus protocol, write to register with control bit in transmission

Data Transfer Recovery

If there is a break in data transmission by !RES or !SCE pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then LDS176 will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (!SCE) is next activated after !RES have been High state. See the following example (See ***Fig. 5.1.9)***

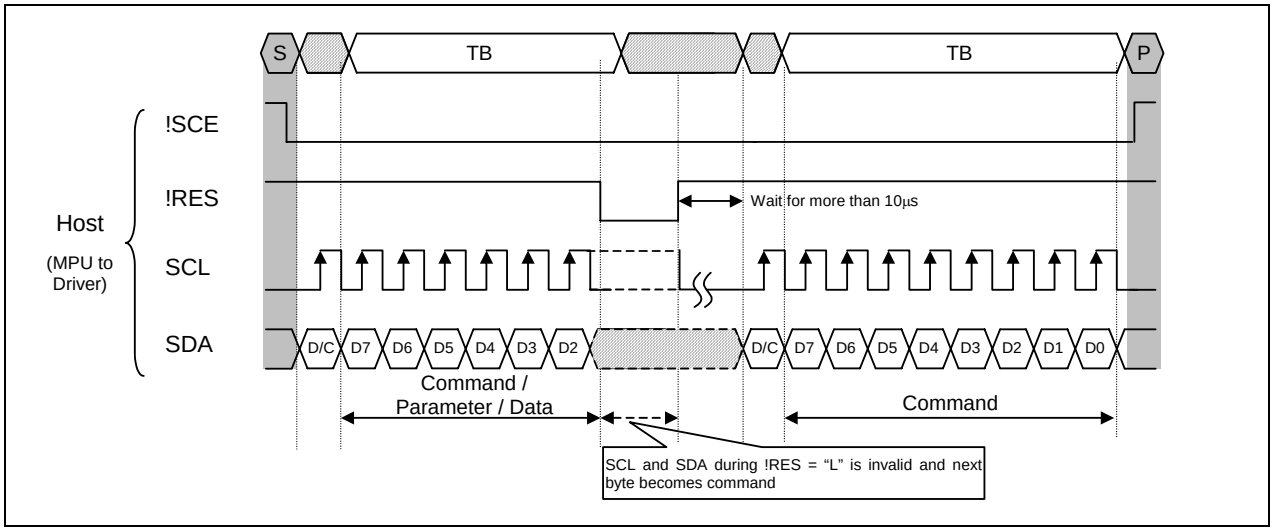


Fig. 5.1.9 Serial bus protocol, write mode – interrupted by !RES

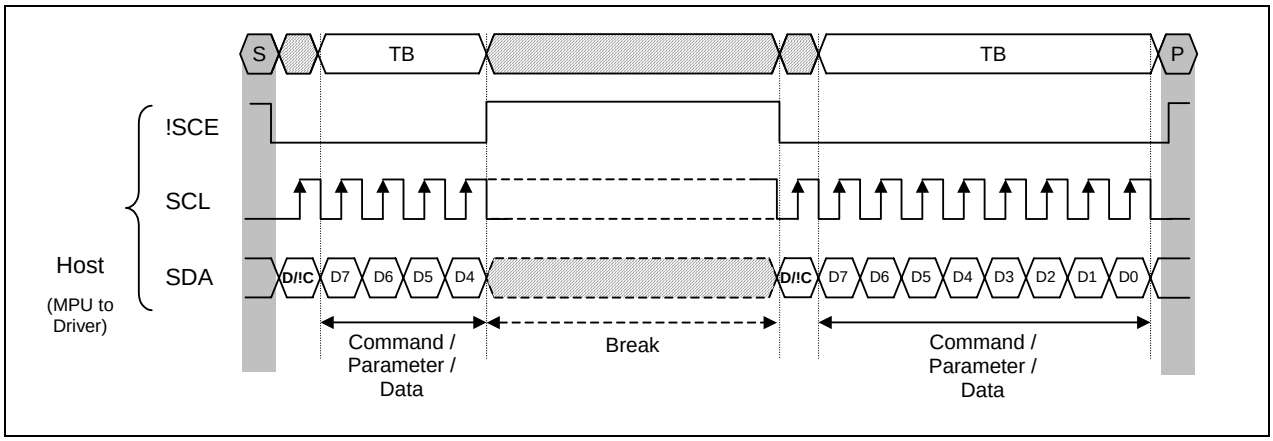


Fig. 5.1.10 Serial bus protocol, write mode – interrupted by !SCE

If 1, 2 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown

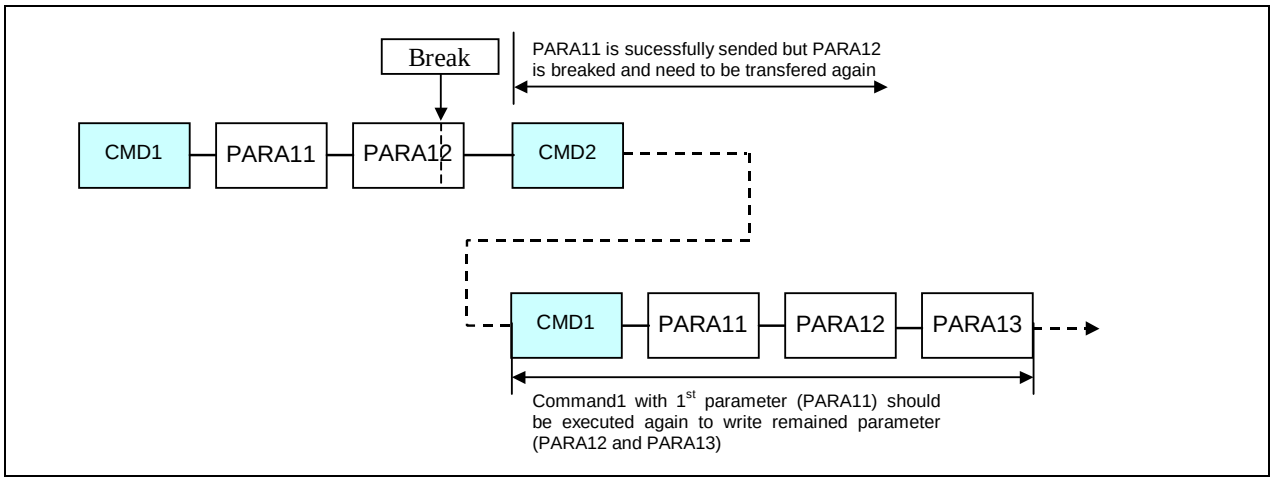


Fig. 5.1.11 Write interrupt recovery

5.1.6 Interface Pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then LDS176 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

This applies to the following 4 conditions:

1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

5.1.6.1 Parallel Interface Pause

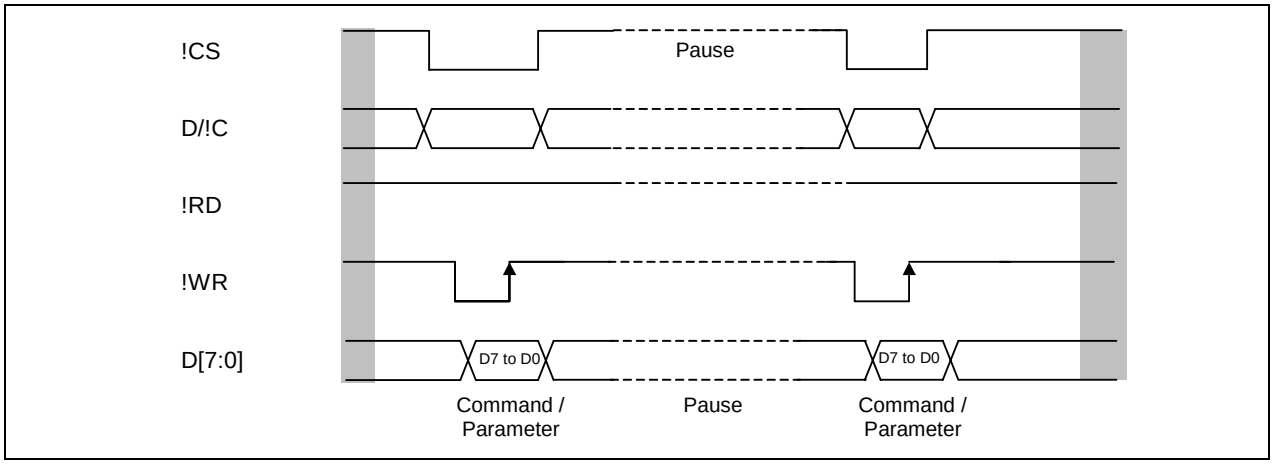


Fig. 5.1.12 Parallel bus protocol, write mode – paused by !SCE

5.1.6.2 Serial Interface Pause

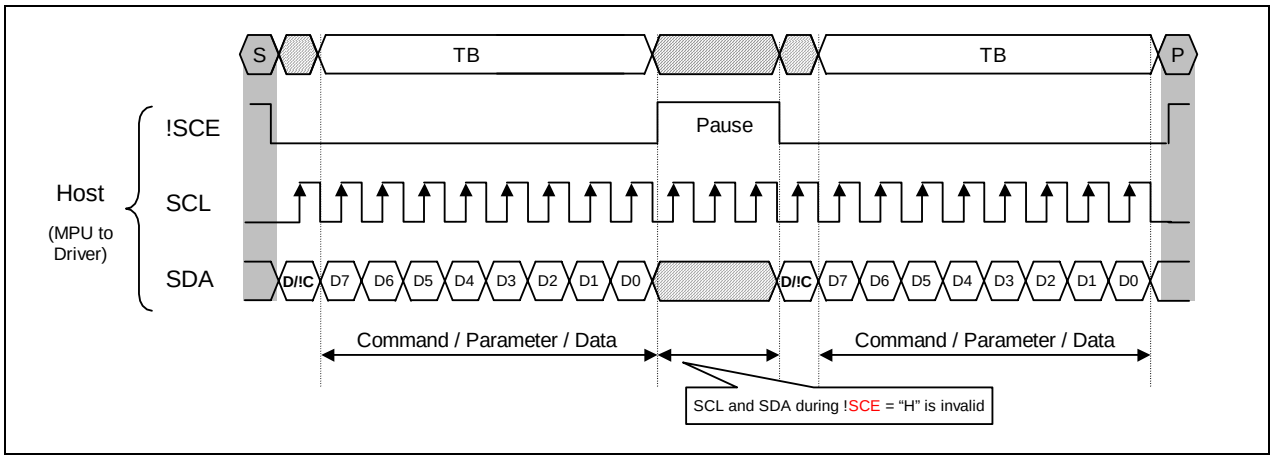


Fig. 5.1.13 Serial bus protocol, write mode – paused by !SCE

5.1.6.3 Read Mode

The read mode of the interface means that the micro controller reads register value from the LDS176. To do so the micro controller first has to send a command (Read ID or Read Register command) and then the following byte is transmitted in the opposite direction. After that !SCE is required to go high before a new command is send (see ***Fig. 5.1.14***).
The LDS176 samples the SDA (input data) at the rising edges, but shifts SDA (output data) at the falling SCL edges with some delay (see AC characteristics section). Thus the micro controller is supported to read data at the rising SCL edges.
After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling SCL edge of the last bit (see ***Fig. 5.1.14).***

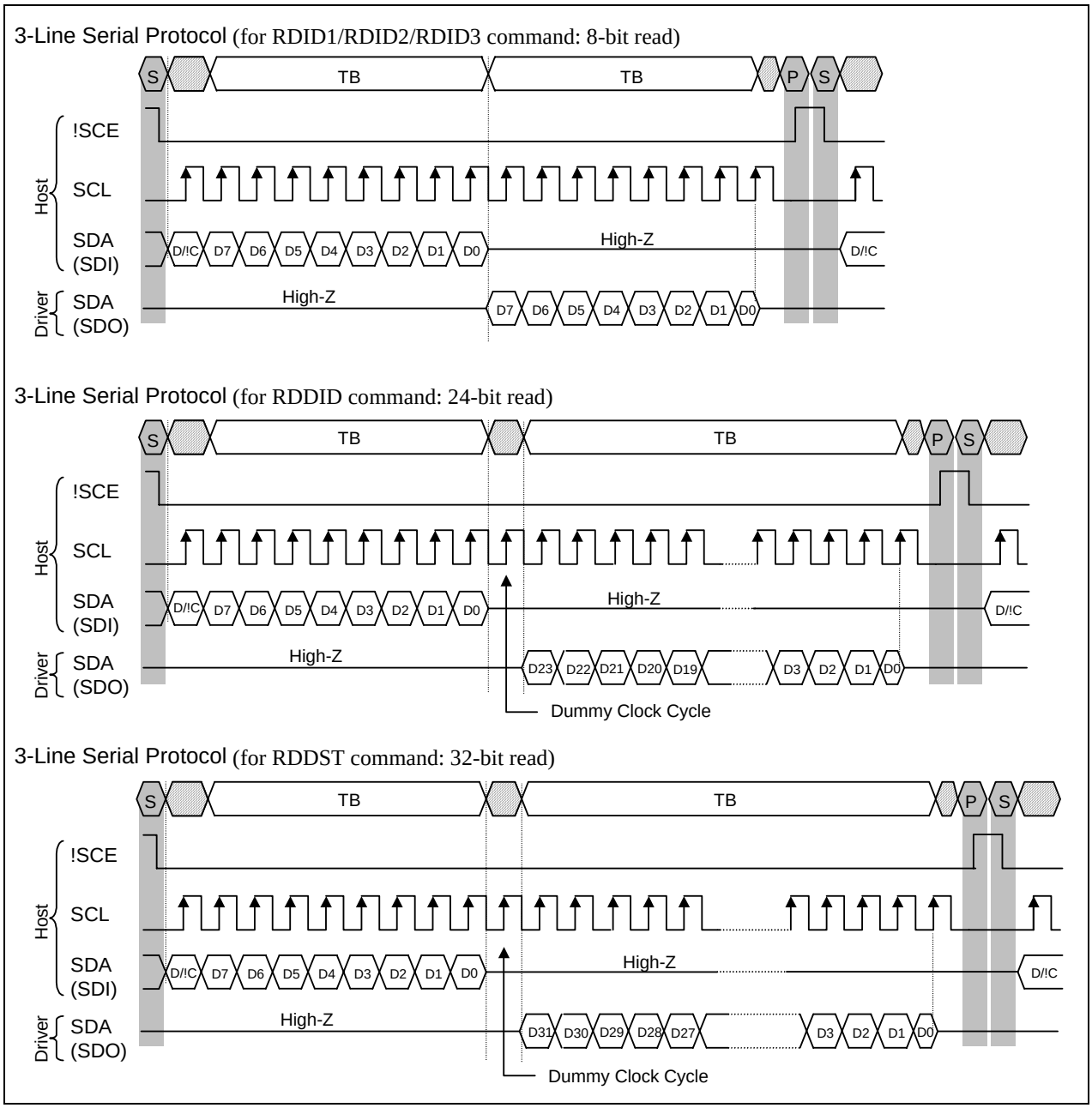


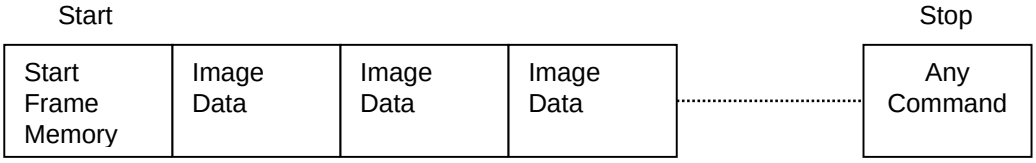
Fig. 5.1.14 Serial bus protocol, read mode

5.1.7 Display Module Data Transfer Modes

The Module has three kinds color modes for transferring data to the display RAM. These are 8-bit color per pixel, 12-bit color per pixel and 16-bit color per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

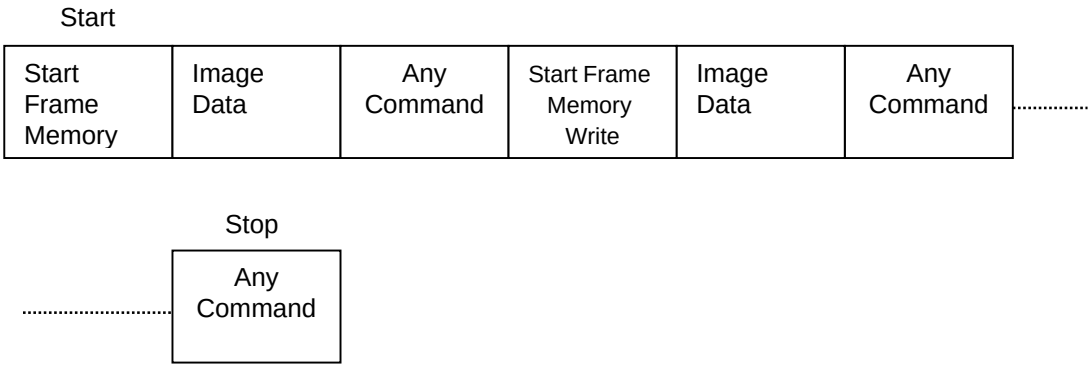
5.1.7.1 Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.



5.1.7.2 Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.



Note:

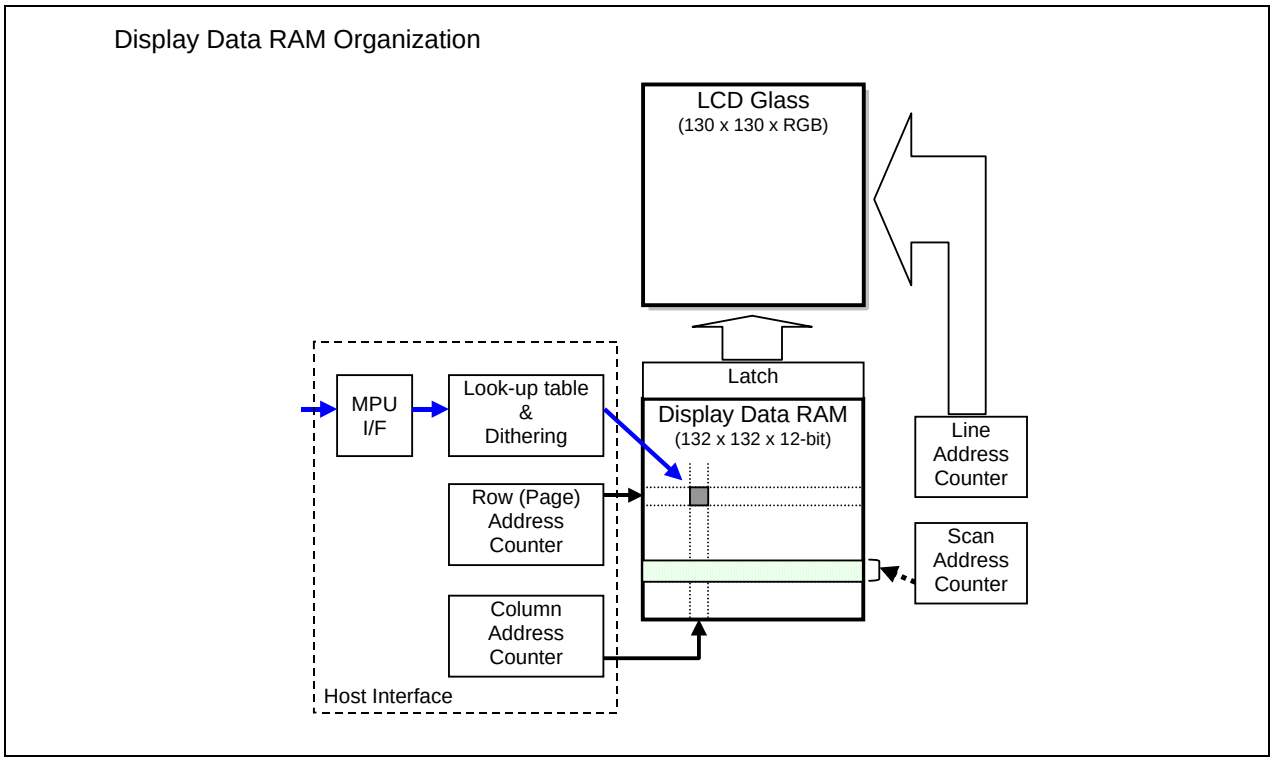
1) These apply to all Data Transfer Color modes on both Serial and Parallel interfaces.

2) The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.

5.2 DISPLAY DATA RAM (DDRAM)

The LDS176 has an integrated 132x132x12-bit graphic type static RAM. This 209k-bit memory allows to store on-chip a 132x132 (RGB) image with a 12-bpp resolution (4k-color).

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Write to the same location of the Frame Memory.



5.2.1 Display Data Formats

Different display data formats are available for three color depth supported by the LDS176 listed below.

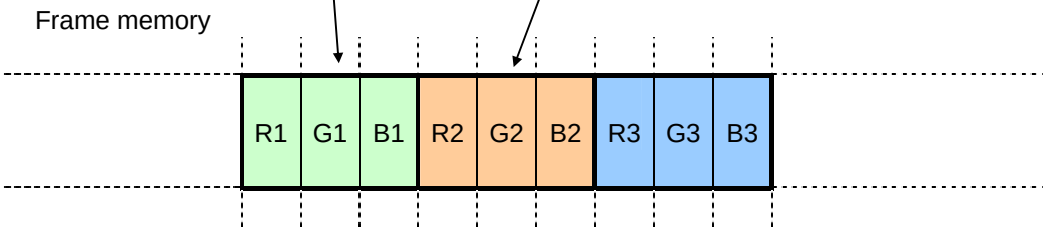
4k colors, RGB 4-4-4-bits input (see ***Table 5.2.1*** and ***Table 5.2.2***)

256 colors, RGB 3-3-2-bits input (see ***Table 5.2.3***)

65k colors, RGB 5-6-5-bits input (see ***Table 5.2.4***)

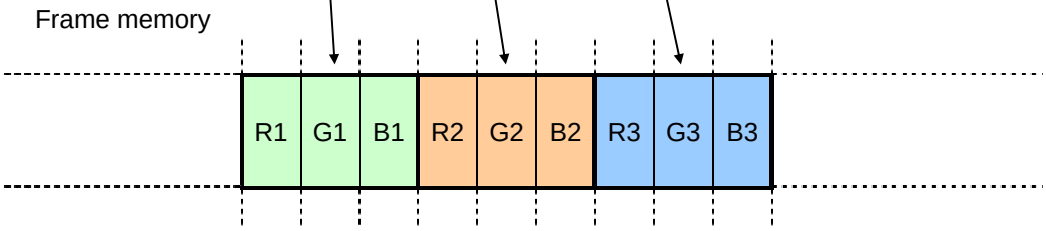
Table 5.2.1 Write data for RGB 4-4-4-bits input (Type A)

4k Color data	D/!C	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	Memory Write Command Code								-
1st write	1	$R1_3$	$R1_2$	$R1_1$	$R1_0$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	-
2nd write	1	$B1_3$	$B1_2$	$B1_1$	$B1_0$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	1st pixel data write (R1/G1/B1)
3rd write	1	$G2_3$	$G2_2$	$G2_1$	$G2_0$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel data write (R2/G2/B2)



4k Color data	D/!C	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	Memory Write Command Code								-
1st write	1	$R1_3$	$R1_2$	$R1_1$	$R1_0$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	-
2nd write	1	$B1_3$	$B1_2$	$B1_1$	$B1_0$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	1st pixel data write (R1/G1/B1)
CMD	0	The other command								Memory write mode terminated
MEMWR	0	Memory Write Command Code								-
1st write	1	$R2_3$	$R2_2$	$R2_1$	$R2_0$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	-
2nd write	1	$B2_3$	$B2_2$	$B2_1$	$B2_0$	$R3_3$	$R3_2$	$R3_1$	$R3_0$	2nd pixel data write (R2/G2/B2)
3rd write	1	$G3_3$	$G3_2$	$G3_1$	$G3_0$	$B3_3$	$B3_2$	$B3_1$	$B3_0$	3rd pixel data write (R3/G3/B3)

$R2_3$ to $R2_0$ of the 1st MEMWR command will be lost and are not used as pixel data.

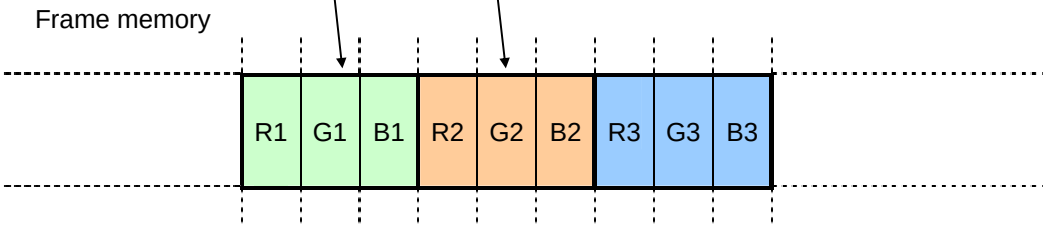


NOTE: 3 bytes are used to transfer 2 pixels or 2 bytes are used to transfer1 pixel with the 12-bit color depth information.
The most significant bits are: Rx_3, Gx_3 and Bx_3.
The least significant bits are: Rx_0, Gx_0 and Bx_0.
Only complete pixels are stored to the frame memory.

Table 5.2.2 Write data for RGB 4-4-4-bits input (Type B)

"X" : Don't care

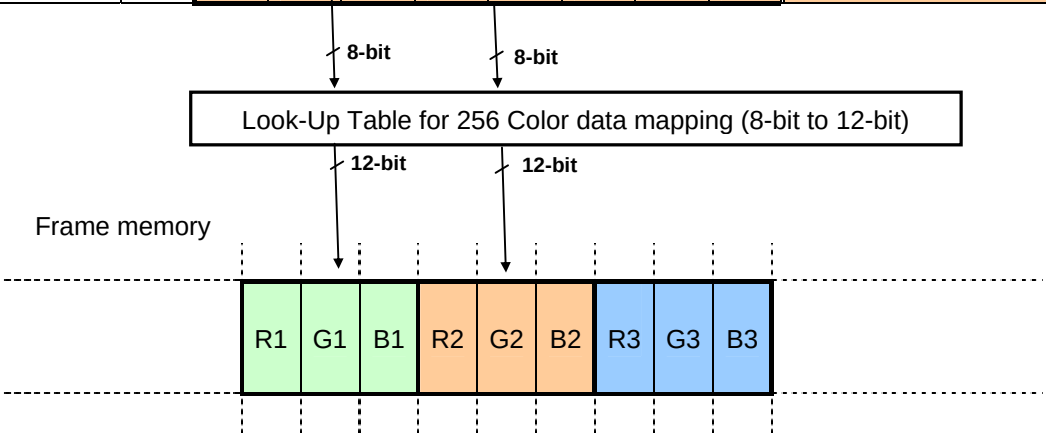
4k Color data	D/!C	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	Memory Write Command Code								-
1st write	1	X	X	X	X	$R1_3$	$R1_2$	$R1_1$	$R1_0$	-
2nd write	1	$G1_3$	$G1_2$	$G1_1$	$G1_0$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	1st pixel data write (R1/G1/B1)
3rd write	1	X	X	X	X	$R2_3$	$R2_2$	$R2_1$	$R2_0$	-
4th write	1	$G2_3$	$G2_2$	$G2_1$	$G2_0$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel data write (R2/G2/B2)



NOTE: 2 bytes are used to transfer 1 pixel with the 12-bit color depth information.
The most significant bits are: Rx_3, Gx_3 and Bx_3.
The least significant bits are: Rx_0, Gx_0 and Bx_0.

Table 5.2.3 Write data for RGB 3-3-2-bits input

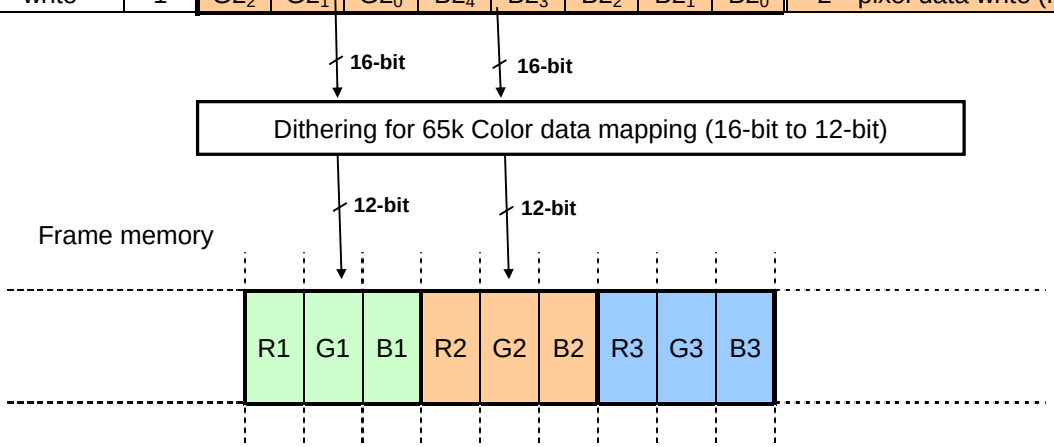
256 Color data	D/!C	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	Memory Write Command Code								-
1st write	1	$R1_2$	$R1_1$	$R1_0$	$G1_2$	$G1_1$	$G1_0$	$B1_1$	$B1_0$	1st pixel data write (R1/G1/B1)
2nd write	1	$R2_2$	$R2_1$	$R2_0$	$G2_2$	$G2_1$	$G2_0$	$B2_1$	$B2_0$	2nd pixel data write (R2/G2/B2)



NOTE: In one byte, 1 pixel is transferred with the 8-bit color depth information.
The most significant bits are: Rx_2, Gx_2 and Bx_1.
The least significant bits are: Rx_0, Gx_0 and Bx_0.

Table 5.2.4 ***Write data for RGB 5-6-5-bits input***

65k Color data	D/!C	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	Memory Write Command Code								-
1st write	1	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	$G1_5$	$G1_4$	$G1_3$	-
2nd write	1	$G1_2$	$G1_1$	$G1_0$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	1st pixel data write (R1/G1/B1)
3rd write	1	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	$G2_5$	$G2_4$	$G1_3$	-
4th write	1	$G2_2$	$G2_1$	$G2_0$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel data write (R2/G2/B2)



NOTE: 2 bytes are used to transfer 1 pixel with the 16-bit color depth information.
The most significant bits are: Rx4, Gx5 and Bx4.
The least significant bits are: Rx0, Gx0 and Bx0.
Only complete pixels are stored to the memory.

5.2.2 Address Counter

The address counter sets the addresses of the display data RAM for writing.

Data is written pixel-wise into the RAM matrix of LDS176. The data for one pixel or two pixels is collected (RGB 4-4-4-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=131 (83hex) and Y=0 to Y=131 (83h). Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined into which will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=131 (83h), YE=131 (83h).

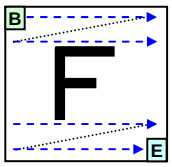
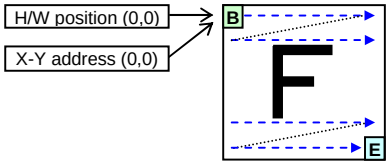
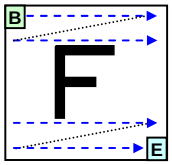
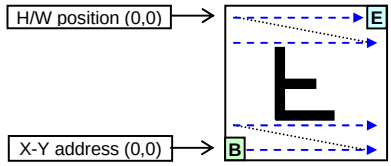
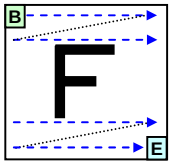
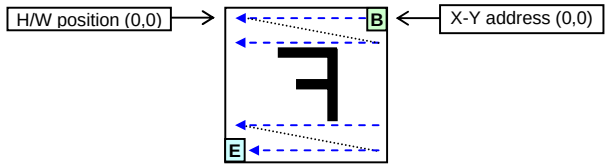
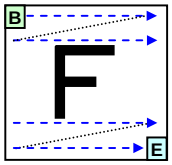
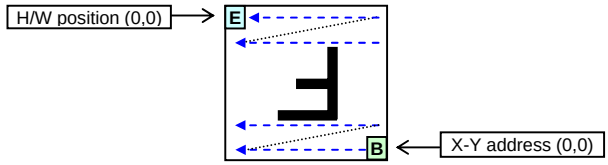
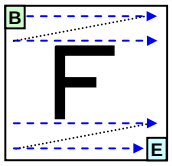
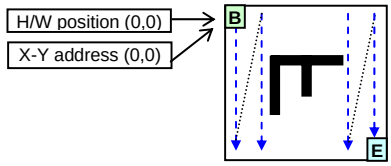
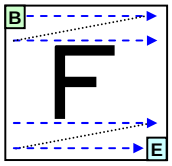
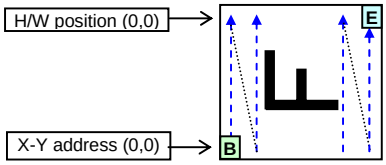
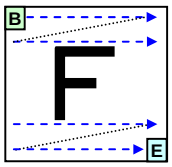
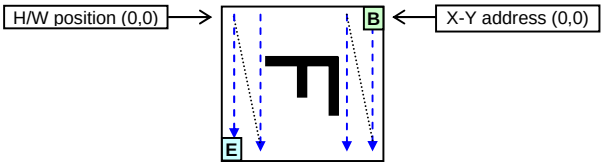
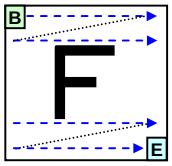
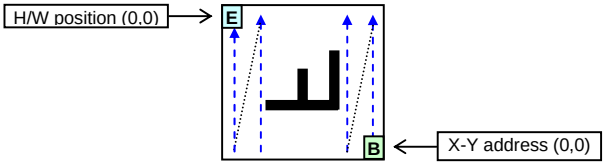
In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET" and "MADCTL (code0) or DATCTL (code1)" (see section "6 INSTRUCTION DESCRIPTION"), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. ***Fig. 5.2.1*** show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as below:

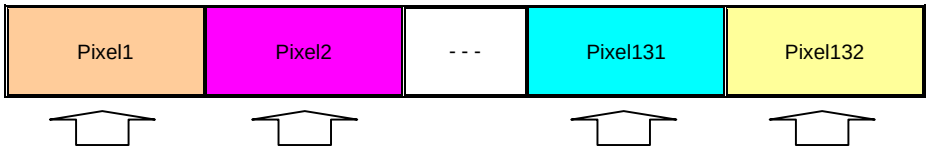
Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

Fig. 5.2.1 Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)

Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

NOTE: MV=D5 parameter of MADCTL command, MX=D6 parameter of MADCTL command, MY=D7 parameter of MADCTL command

5.2.3 Memory Map



SEG Out		S0	S1	S2	S3	S4	S5	- - -	S390	S391	S392	S393	S394	S395		
RA		RGB=0	RGB=1		RGB=0	RGB=1		RGB Order	RGB=0	RGB=1		RGB=0	RGB=1		SA	
MY=0	*MY=1*														*ML=0*	*ML=1*
0	131	R1$_{3-0}$	G1$_{3-0}$	B1$_{3-0}$	R2$_{3-0}$	G2$_{3-0}$	B2$_{3-0}$	- - -	R130$_{3-0}$	G130$_{3-0}$	B130$_{3-0}$	R131$_{3-0}$	G131$_{3-0}$	B131$_{3-0}$	0	131
1	130							- - -							1	130
2	129							- - -							2	129
3	128							- - -							3	128
4	127							- - -							4	127
5	126							- - -							5	126
6	125							- - -							6	125
7	124							- - -							7	124
8	123							- - -							8	123
9	122							- - -							9	122
10	121							- - -							10	121
11	120							- - -							11	120
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
124	7							- - -							124	7
125	6							- - -							125	6
126	5							- - -							126	5
127	4							- - -							127	4
128	3							- - -							128	3
129	2							- - -							129	2
130	1							- - -							130	1
131	0							- - -				RN$_{3-0}$	GN$_{3-0}$	BN$_{3-0}$	131	0
CA	*MX=0*	0			1			- - -	130			131				
	MX=1	131			130			- - -	1			0				

NOTE: RA = Row Address,

CA = Column Address,

SA = Scan Address,

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

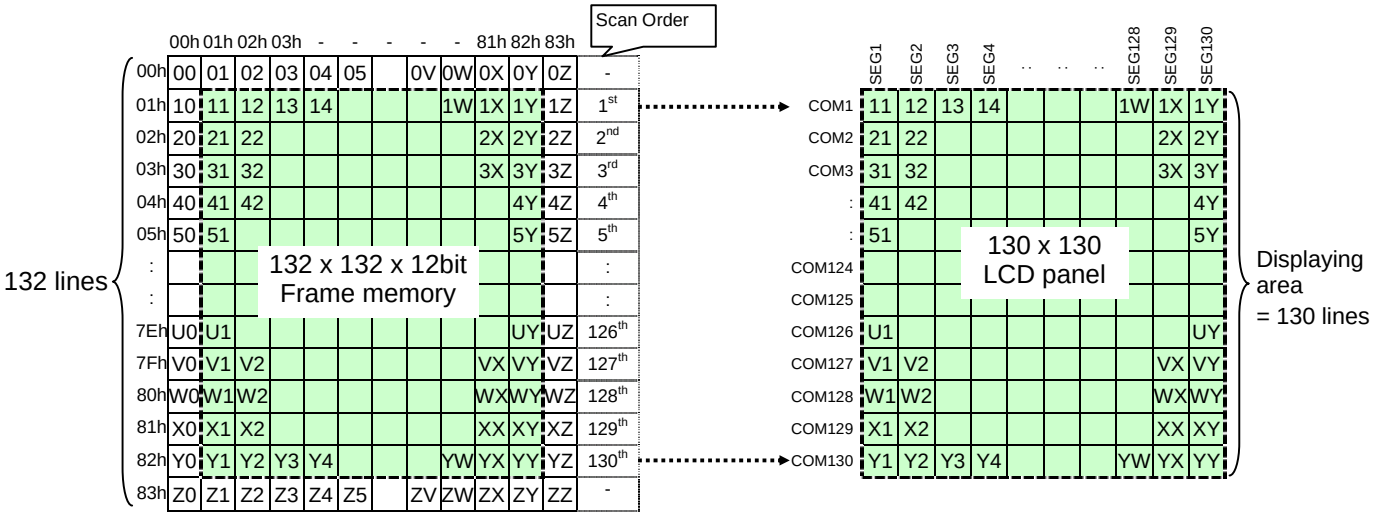
ML = Scan direction parameter, D4 parameter of MADCTL command

RGB= Red, Green and Blue pixel position change, D3 parameter of MADCTL command

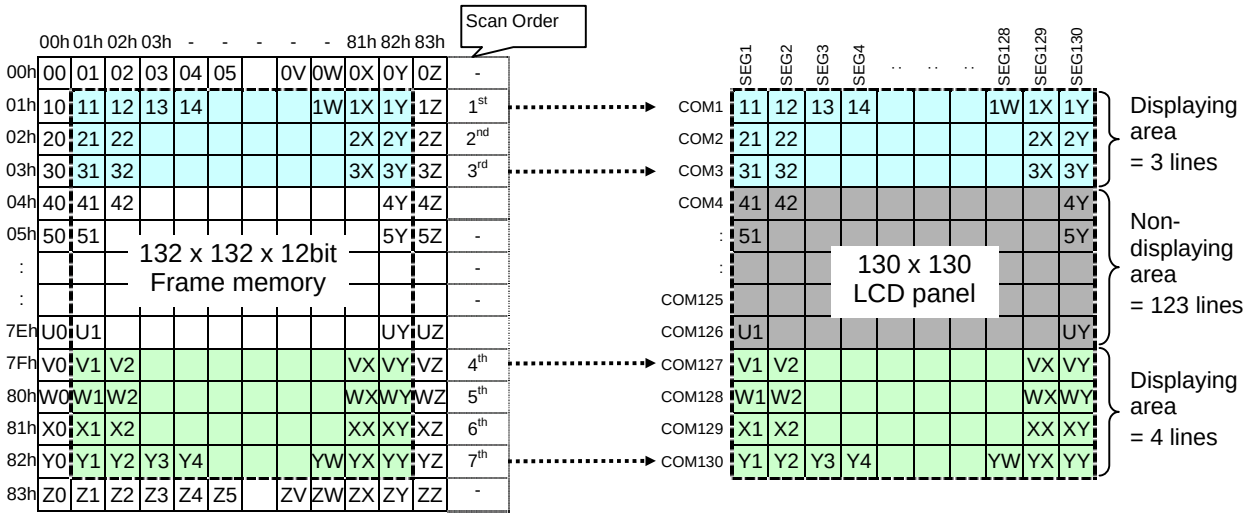
5.2.4 Normal Display On or Partial Mode On, Vertical Scroll Off

In this mode, contents of the frame memory within an area where column pointer is 01h to 82h and page pointer is 01h to 82h is displayed.
To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (1,1).

Example1) Normal Display On



Example2) Partial Display On: PSL [7:0] = 7Fh, PEL [7:0] = 03h, MADCTR (ML)=0



5.2.5 Vertical Scroll

5.2.5.1 Rolling and Non-Rolling Scroll

There are 2 types of vertical scrolling, which are determined by the commands " Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

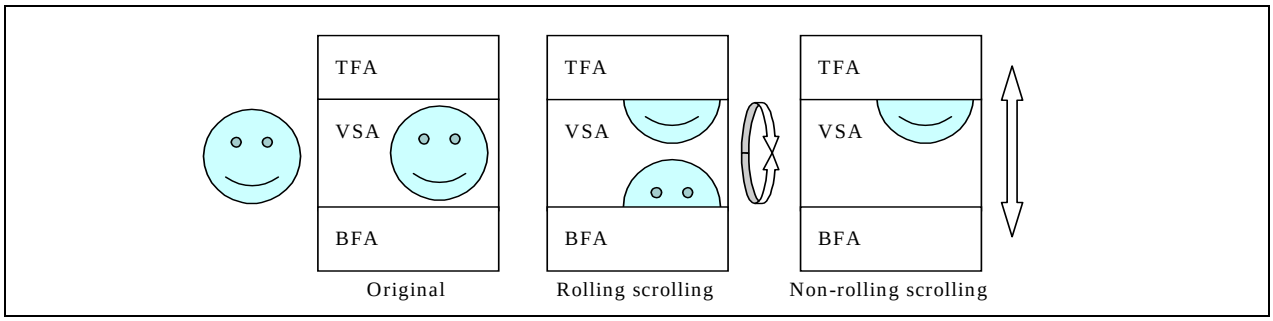
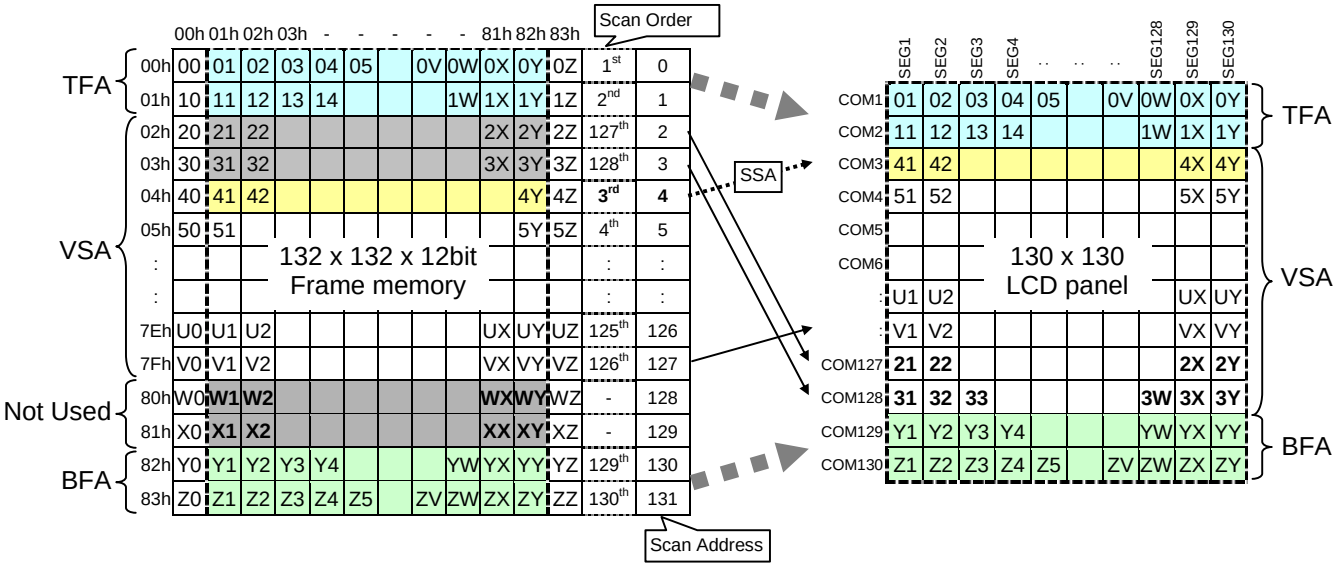


Fig. 5.2.2 Difference between Rolling Scrolling and Non-rolling scrolling

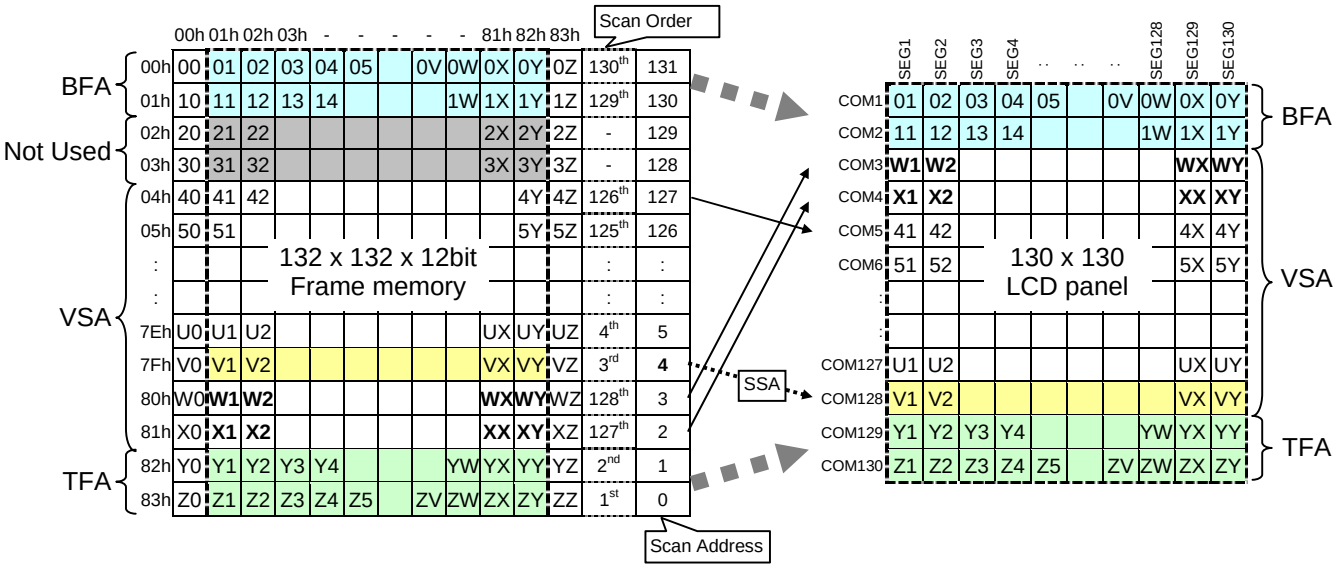
Type 1

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=130. In this case, 'rolling' scrolling is applied as shown below. Not used area (lines) is just over BFA.

Example1) Panel size=130 x 130, TFA =2, VSA=126, BFA=2, SSA=4,
MADCTR (ML)=0: Rolling Scroll



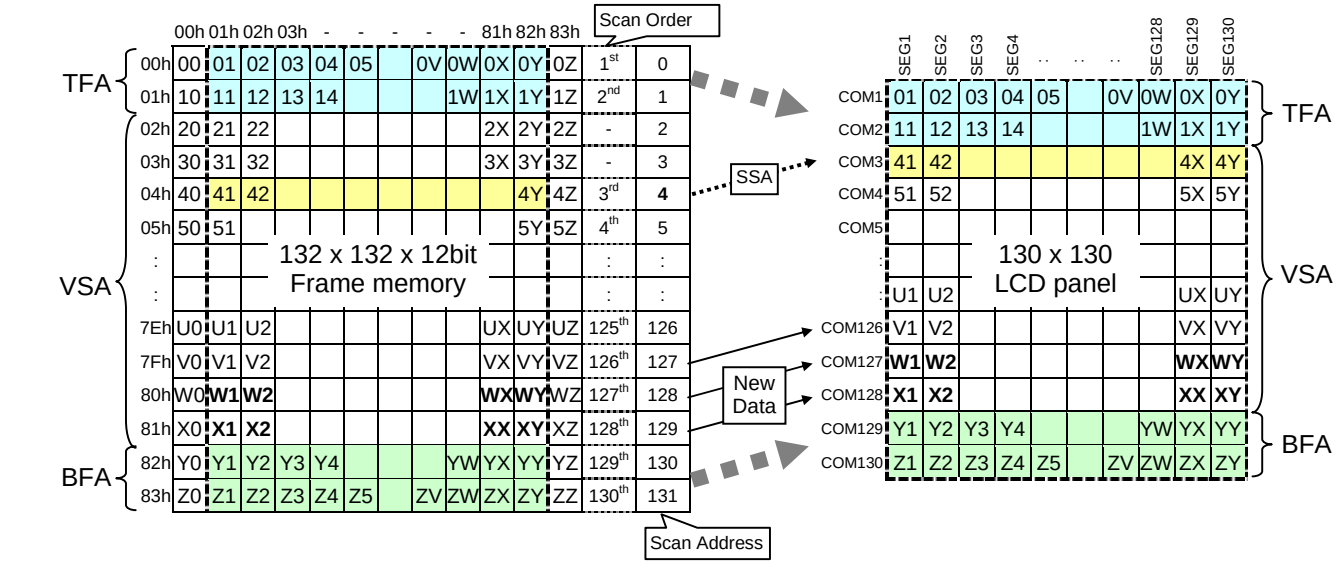
Example2) Panel size=130 x 130, TFA =2, VSA=126, BFA=2, SSA=4,
MADCTR (ML)=1: Rolling Scroll (TFA and BFA are exchanged)



Type 2

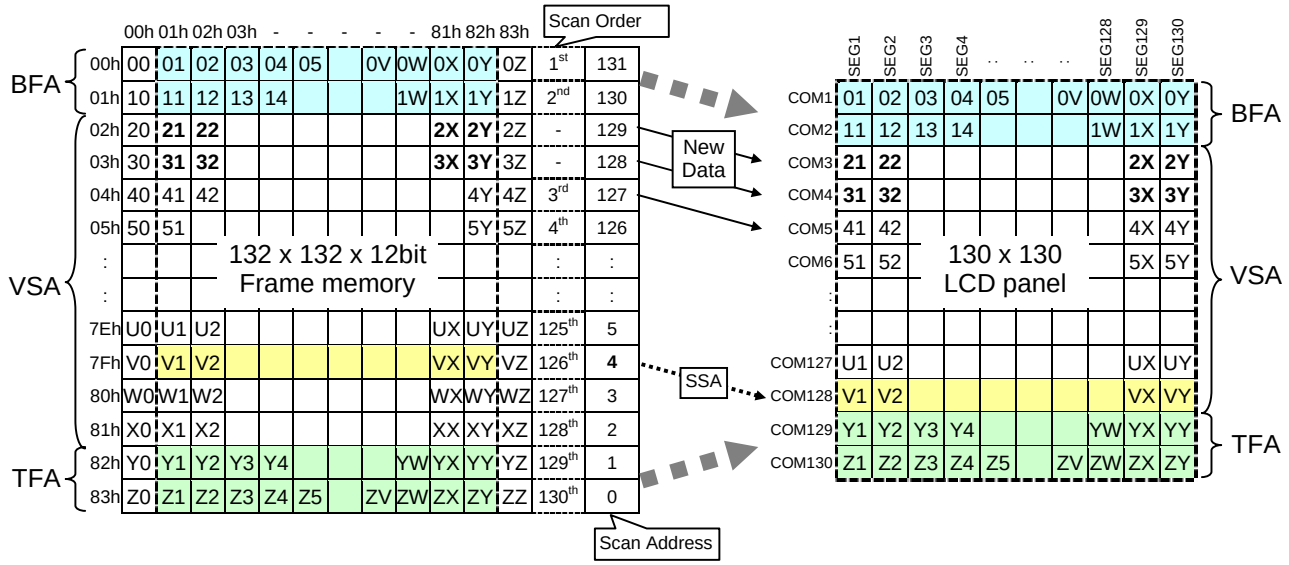
When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) = 131 or 132. In this case, "non-rolling" Scrolling is applied. New data can be written into the "extra memory lines", If (TFA+VSA+BFA)=131 then one line is available for inserting new data. If (TFA+VSA+BFA)=132 then two lines are available for inserting new data.

Example1) Panel size=130 x 130, TFA =2, VSA=128, BFA=2, SSA=4,
MADCTR (ML)=0: Non-Rolling Scroll



Note: In this example it was assumed that prior to sending the Vertical Scrolling Start Address, "New Data" had been written to the Frame Memory in the area described and the Vertical Scrolling Start Address was (Current Position-2Lines).

Example2) Panel size=130 x 130, TFA =2, VSA=128, BFA=2, SSA=4,
MADCTR (ML)=1: Non-Rolling Scroll (TFA and BFA are exchanged)



5.2.5.2 Vertical Scroll Example

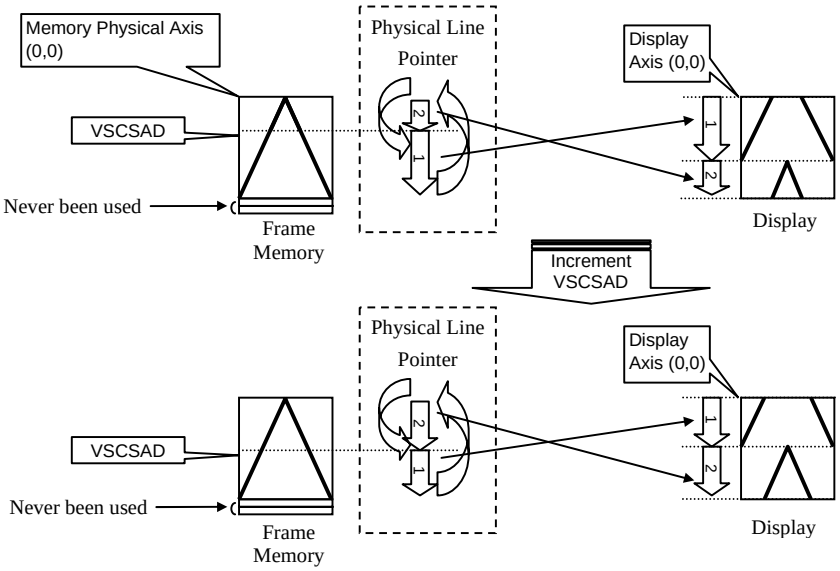
There are 2 types of vertical scrolling, which are determined by the commands " Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

Case 1: TFA + VSA + BFA<130

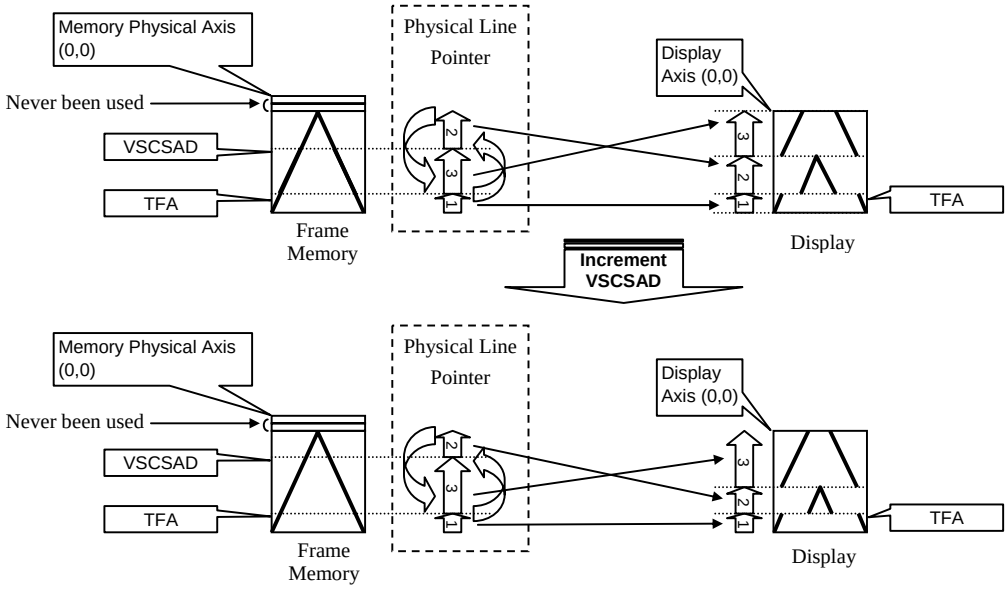
N/A. Do not set TFA + VSA + BFA<130. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=130 (Rolling Scrolling)

Example1) When MADCTR parameter ML="0", TFA=0, VSA=130, BFA=0 and VSCSAD=40.

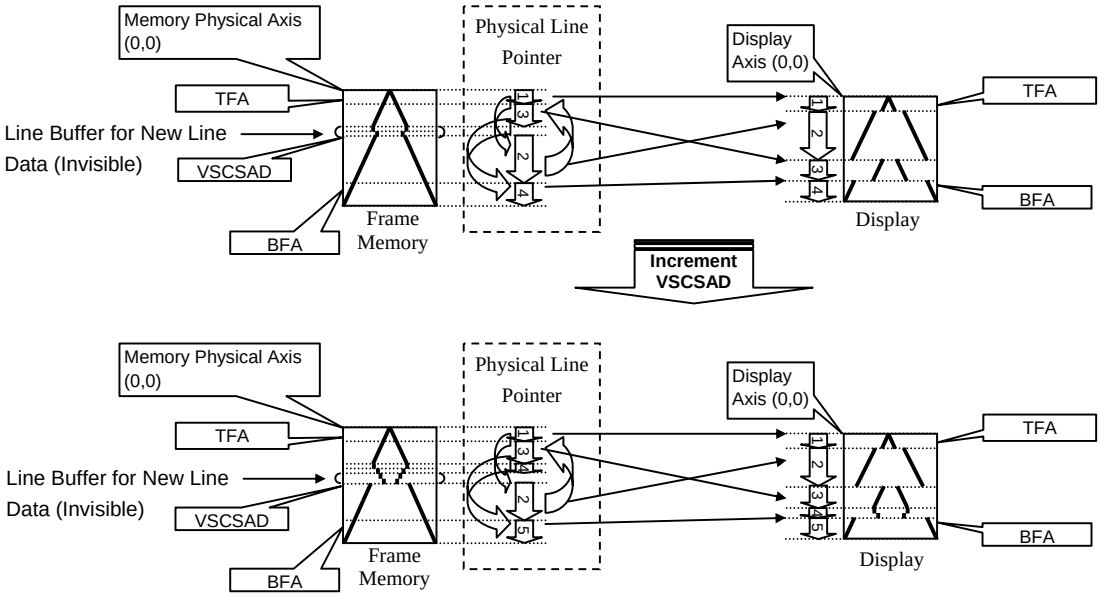


Example2) When MADCTR parameter ML="1", TFA=30, VSA=100, BFA=0 and VSCSAD=80.



Case3: TFA + VSA + BFA =132 (Scrolling with 2line buffer)

Example) When MADCTR parameter ML="0", TFA=20, VSA=82, BFA=30 and VSCSAD=60.



5.2.6 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

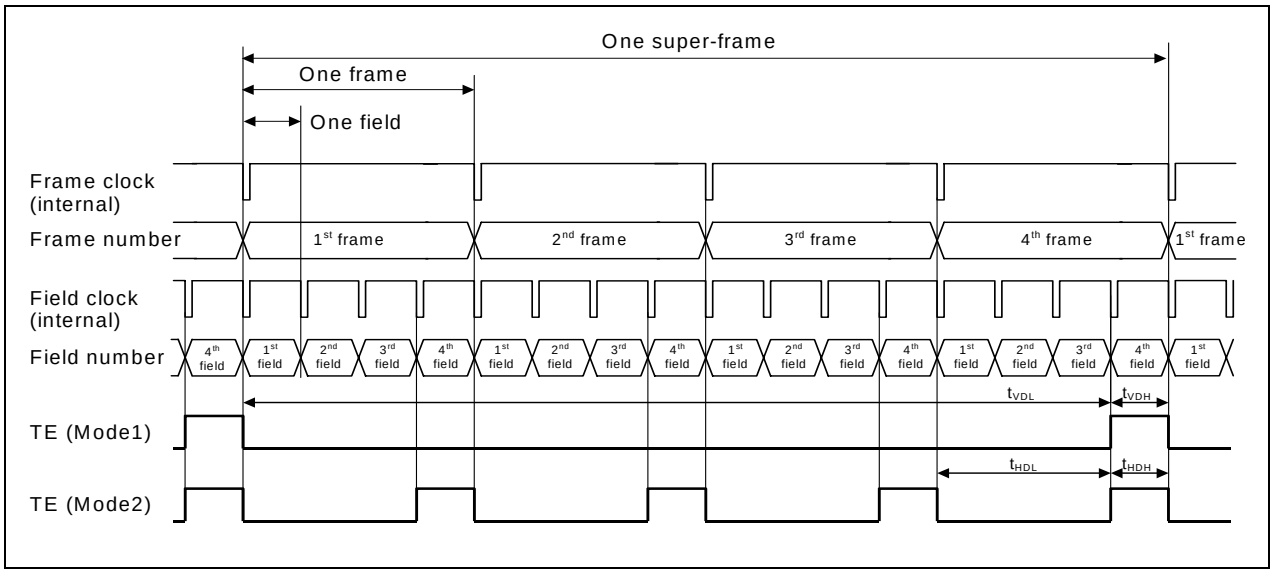
5.2.6.1 Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Sync (t_{VHD}) information only before Super-frame's start (only during every 4th frame and every 4th field).

t_{vdh} = The LCD display is updating the end (4th frame) of the previous Super-frame from the Frame memory
t_{vdl} = The LCD display is updated 1st, 2nd and 3rd frames (It is possible that the begin of the 4th frame is also included for this timing) from the Frame Memory.

Mode 2, the Tearing Effect Output signal consists of only H-Sync (1 frame) information, there is one high pulse and 1 low pulse during every frame.

t_{hdh} = The LCD display is updated the end of the frame field from the Frame Memory.
t_{hdl} = The LCD display is updated the begin of the frame field from the Frame Memory.



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

5.2.6.2 Tearing Effect Line Timing

The Tearing Effect signal is described below:

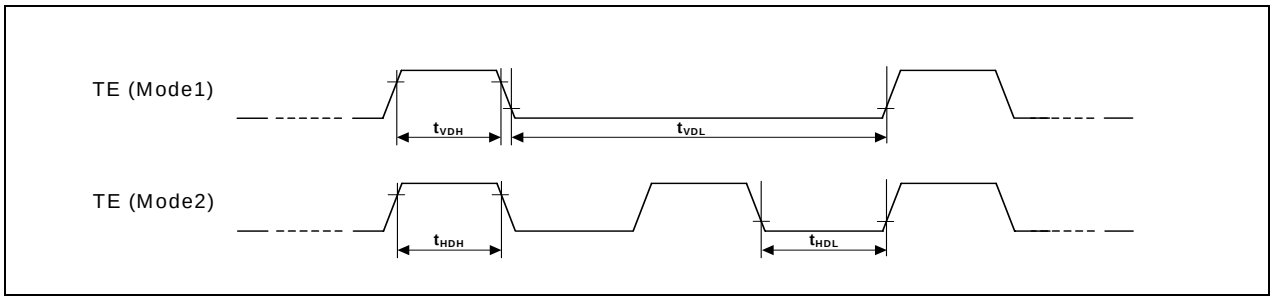


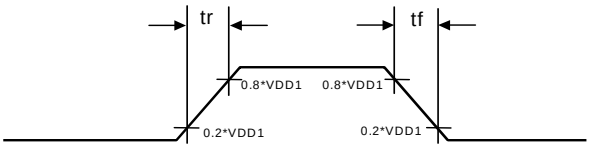
Table 5.2.5 AC characteristics of Tearing Effect Signal

Idle Mode Off (Frame Rate = 100Hz)

Symbol	Parameter	min	max	unit	description
t_{VDL}	Vertical Timing Low Duration	37.5	-	ms	Mode1
t_{VDH}	Vertical Timing High Duration	2.5	-	ms	
t_{HDL}	Horizontal Timing Low Duration	7.5		ms	Mode2
t_{HDH}	Horizontal Timing High Duration	2.5		ms	

NOTE: The timings in Table 5.2.5 apply when MADCTL B4=0 and B4=1

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



5.2.7 Colour Depth Conversion Look Up Tables

Color	Look Up Table Outputs Frame Memory Data (4-bit)	RGBSET parameter	Look Up Table Inputs 256 Color Data
RED	R_{003} R_{002} R_{001} R_{000}	1	000
	R_{013} R_{012} R_{011} R_{010}	2	001
	R_{023} R_{022} R_{021} R_{020}	3	010
	R_{033} R_{032} R_{031} R_{030}	4	011
	R_{043} R_{042} R_{041} R_{040}	5	100
	R_{053} R_{052} R_{051} R_{050}	6	101
	R_{063} R_{062} R_{061} R_{060}	7	110
	R_{073} R_{072} R_{071} R_{070}	8	111
GREEN	G_{003} G_{002} G_{001} G_{000}	9	000
	G_{013} G_{012} G_{011} G_{010}	10	001
	G_{023} G_{022} G_{021} G_{020}	11	010
	G_{033} G_{032} G_{031} G_{030}	12	011
	G_{043} G_{042} G_{041} G_{040}	13	100
	G_{053} G_{052} G_{051} G_{050}	14	101
	G_{063} G_{062} G_{061} G_{060}	15	110
	G_{073} G_{072} G_{071} G_{070}	16	111
BLUE	B_{003} B_{002} B_{001} B_{000}	17	00
	B_{013} B_{012} B_{011} B_{010}	18	01
	B_{023} B_{022} B_{021} B_{020}	19	10
	B_{033} B_{032} B_{031} B_{030}	20	11

5.3 INSTRUCTION DECODER & REGISTER

The instruction decoder identifies command words arriving at the interface and routes the following data type bytes to their destination. The command set can be found in “6 INSTRUCTION DESCRIPTION” section.

5.4 GRAY SIGNAL GENERATOR

As grayscale driving scheme the frame rate control (FRC) with carefully controlled mixing of the FRC pattern on each pixel and pulse width modulation (PWM) is used. The special mixing assures that the pattern placed on each pixel is different to each of its neighbors. In the Frame Rate Control 4 frames form a super frame. All 4 frames have the same duration.

5.5 GRAY SELECTOR

This block selects gray signal from gray signal generator block according to the display data RAM outputs.

5.6 SYSTEM CLOCK GENERATOR

The timing generator produces the various signals to drive the internal circuitry. Internal chip operation is not affected by operations on the data bus.

5.7 OSCILLATOR

LDS176 has on-chip oscillator which does not require external components. This oscillator output signal is used for system clock generation for internal display operation

5.8 SEGMENT DRIVER

The segment driver section includes 132x3 column outputs (S0 to S395), which should be connected directly to the LCD. The segment output signals are generated in the data processing block after the data is read out of the RAM and after processing with the appropriate orthogonal function, which represent the simultaneous selected rows. When less then 396 segments are required the unused segment outputs should be left open-circuit.

5.9 BLOCK COUNTER

This counter counts common signal block, which is composed of concurrently selected line.

5.10 COMMON DRIVER

The row driver section includes 132 row outputs (C0 to C131) which should be connected directly to the LCD.

5.11 LCD POWER GENERATION CIRCUIT

5.11.1 LCD Power Generation Scheme

LCD power circuit generates voltages required to drive liquid crystal. The power circuit consists of booster circuits (booster1, booster2 and booster3), voltage regulators (regulator1 and regulator2) and voltage followers. Each circuit can be turn on or off separately by command (command code 1, PWRCNT) or concurrently by command (command code 2, BSTROFF/BSTRON).

LCD power generation scheme is illustrated in ***Fig. 5.11.1.***

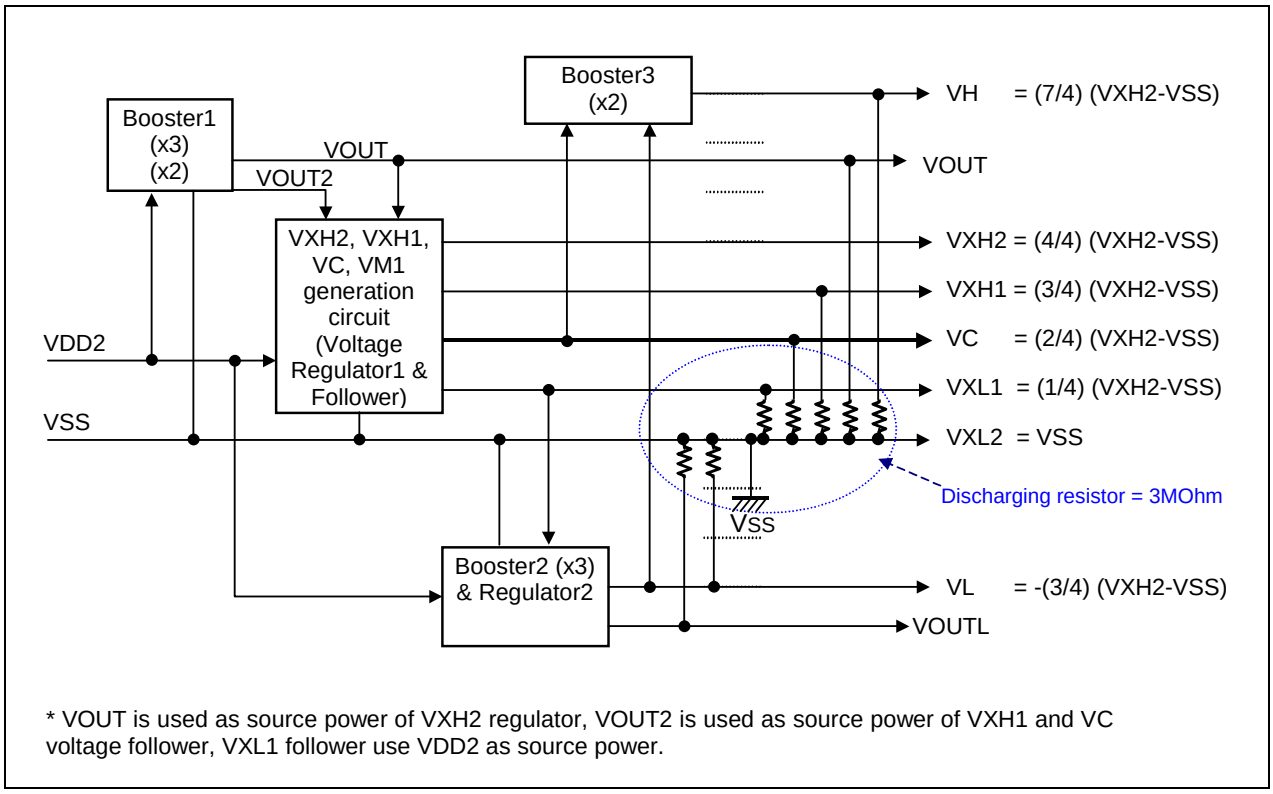


Fig. 5.11.1 LCD power generation scheme

5.11.2 Booster1 Circuit

Booster1 circuit triples the voltage of VDD2-VSS and the boosted voltage is output at VOUT pin.

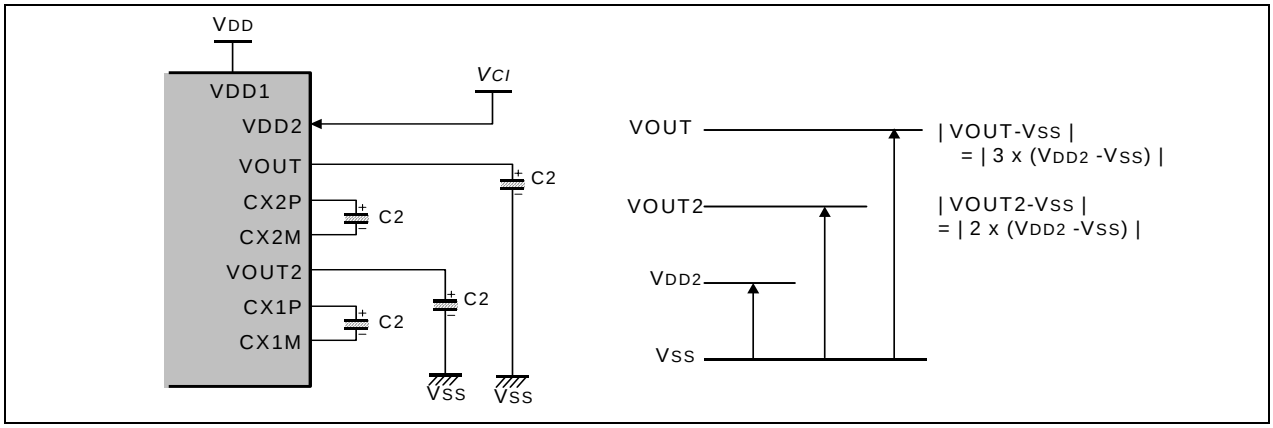


Fig. 5.11.2 LCD power generation scheme

5.11.3 Voltage Regulator1 Circuit

5.11.3.1 Voltage Regulator1 Circuit

Voltage regulator1 circuit generates the liquid crystal drive voltage VXH2 using VOUT from the booster1 circuit. LDS176 incorporates the high-precision constant voltage source, 64-step electronic volume control function and resister to regulate VXH2 voltage. The voltage regulator circuit covers a wider temperature range with ROM look-up table function.

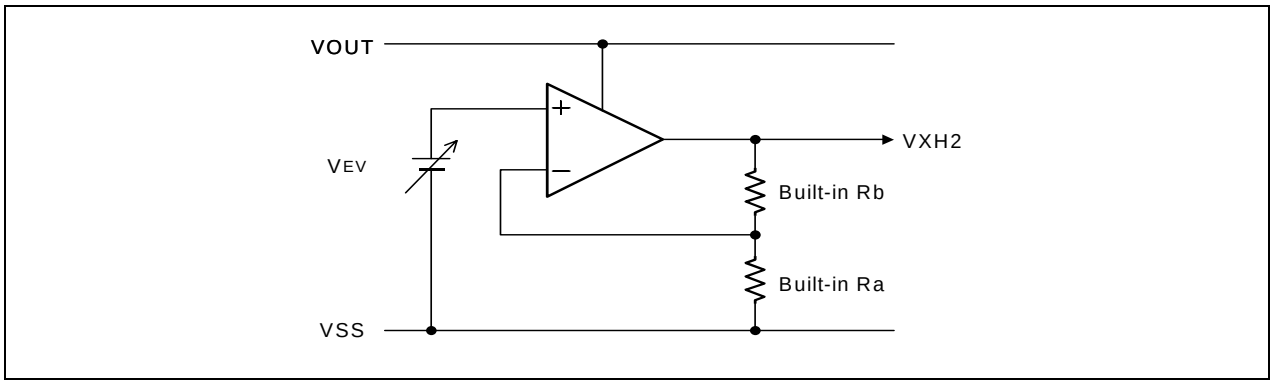


Fig. 5.11.3 Voltage regulator1 circuit (with built-in Ra and Rb)

5.11.3.2 Built-in Resistor for VXH2 Voltage Regulation

Using this resistor and the electronic volume control function allows you to control the liquid crystal drive voltage VXH2 to an optimum level for the LCD panel with the command alone, without resorting to external resistors.

VXH2 output voltage can be determined from [Equation1] as long as the relation VXH2 < VOUT is met.

$VXH2 = (1 + Rb/Ra) * V_{EV} = (1 + Rb/Ra) * (1 – (\alpha+2*2)/218*2) * V_{REG}$ [Equation1]

V_{REG} = 1.6V (Typ.) at Temp = 25°C constant voltage source

Rb/Ra in [Equation1] is the resistance ratio of the built-in VXH2 voltage-regulating resistance. This ratio can be varied in 8 levels by changing parameter RR [2:0] of electronic volume control command. Reference ratios of "1+Rb/Ra" are shown in ***Table 5.11.1***.

Table 5.11.1 Resistance Ratio according to the Parameter RR [2:0]

RR2	RR1	RR0	1 + Rb/Ra	VXH2 voltage value
0	0	0	2.9032	Small
0	0	1	3.1914	↑
0	1	0	3.4090	|
0	1	1	3.6585	|
1	0	0	3.8793	|
1	0	1	4.0909	|
1	1	0	4.3269	↓
1	1	1	4.5454	Large

5.11.3.3 Constant Voltage Source and Electronic Volume Control Circuit

The constant voltage generates VREG - the reference voltage inside the IC.

The electronic volume control circuit varies α in [Equaion1] according to parameters EV [6:0] of electronic volume control command and offset value (EOF [4:0]) read from EEPROM (for the relationship between EV, EOF and EV_IN, see section "6.1.41"). ***Table 5.11.2*** lists relationship between EV_IN [6:0] and α.

Table 5.11.2 Relationship between EV_IN [6:0] and α

EV_IN6	EV_IN5	EV_IN4	EV_IN3	EV_IN2	EV_IN1	EV_IN0	α	VXH2 voltage value
0	0	0	0	0	0	0	127	Small
0	0	0	0	0	0	1	126	↑
0	0	0	0	0	1	0	125	|
0	0	0	0	0	1	1	125	|
:	:	:	:	:	:	:	:	|
:	:	:	:	:	:	:	:	|
1	1	1	1	1	0	0	3	|
1	1	1	1	1	0	1	2	|
1	1	1	1	1	1	0	1	↓
1	1	1	1	1	1	1	0	Large

5.11.4 Voltage Divider & Voltage Follower Circuit

The voltage divider & follower circuit generates driving voltage VXH1, VC and VXL1 from regulator output VXH2.

VXH1 = (3/4) VXH2
VC = (2/4) VXH2
VXL1 = (1/4) VXH2

5.11.5 Booster2 Circuit

The booster2 circuit triples the voltage of VDD2-VSS to the negative direction and the boosted voltage is output at VOUTL pin.

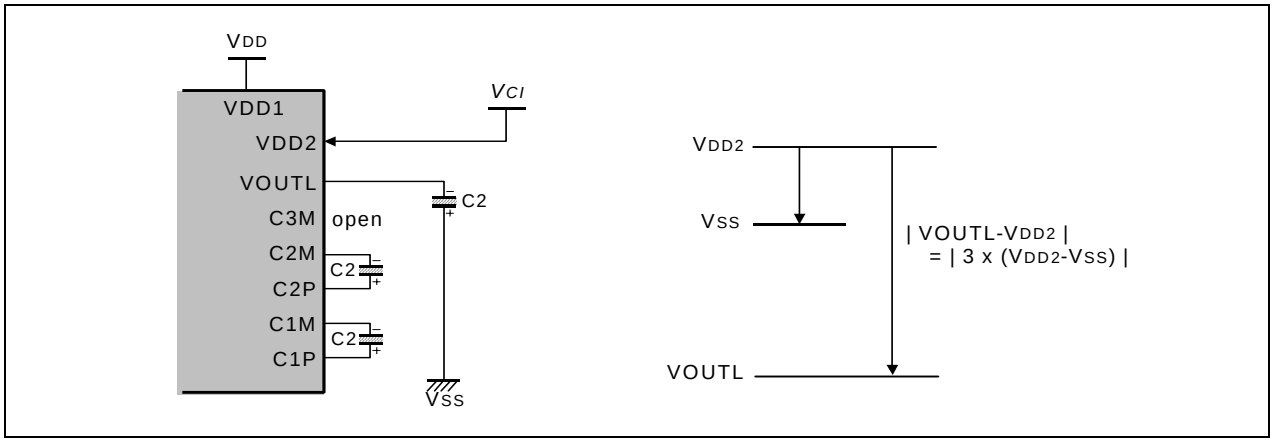


Fig. 5.11.4 Booster2 circuit external cap connection

5.11.6 Voltage Regulator2 Circuit

The voltage regulator2 circuit generates the liquid crystal drive voltage VL using VOUTL as power and VXL1 as reference voltage.

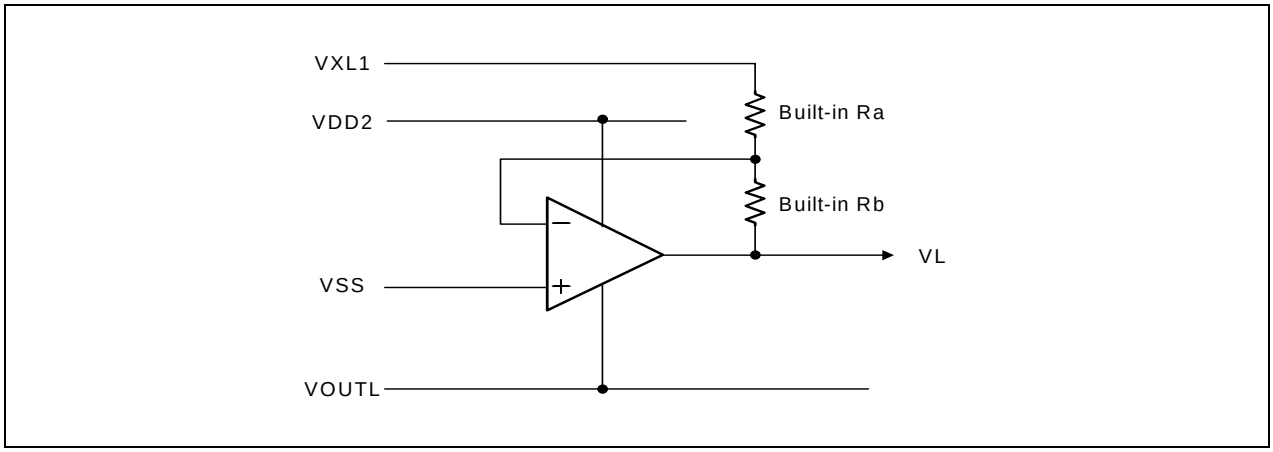


Fig. 5.11.5 Voltage regulator2 circuit

5.11.7 Booster3 Circuit

The booster3 circuit doubles the voltage of VL-VC to the positive direction and the boosted voltage is used as liquid crystal drive voltage VH.

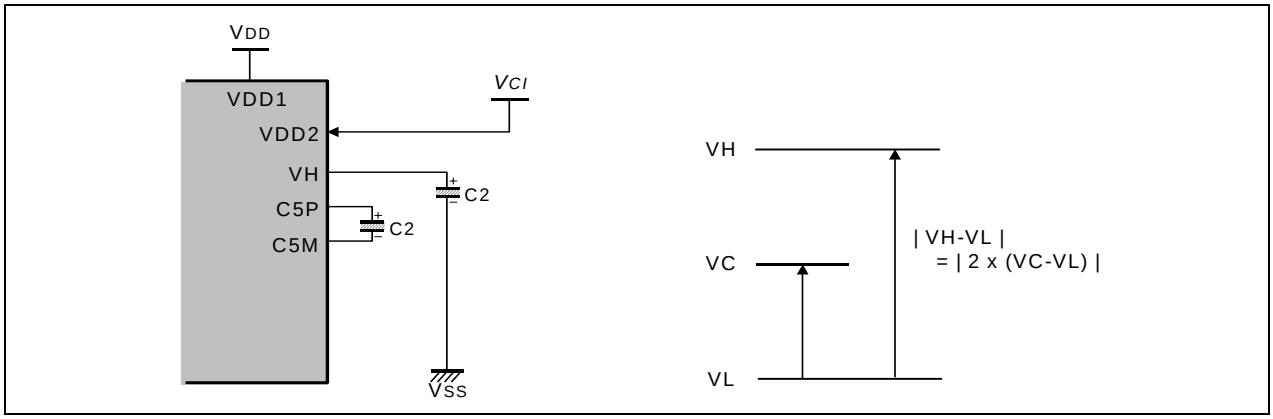


Fig. 5.11.6 Booster3 circuit external cap connection

5.11.8 Power Circuit Application Example

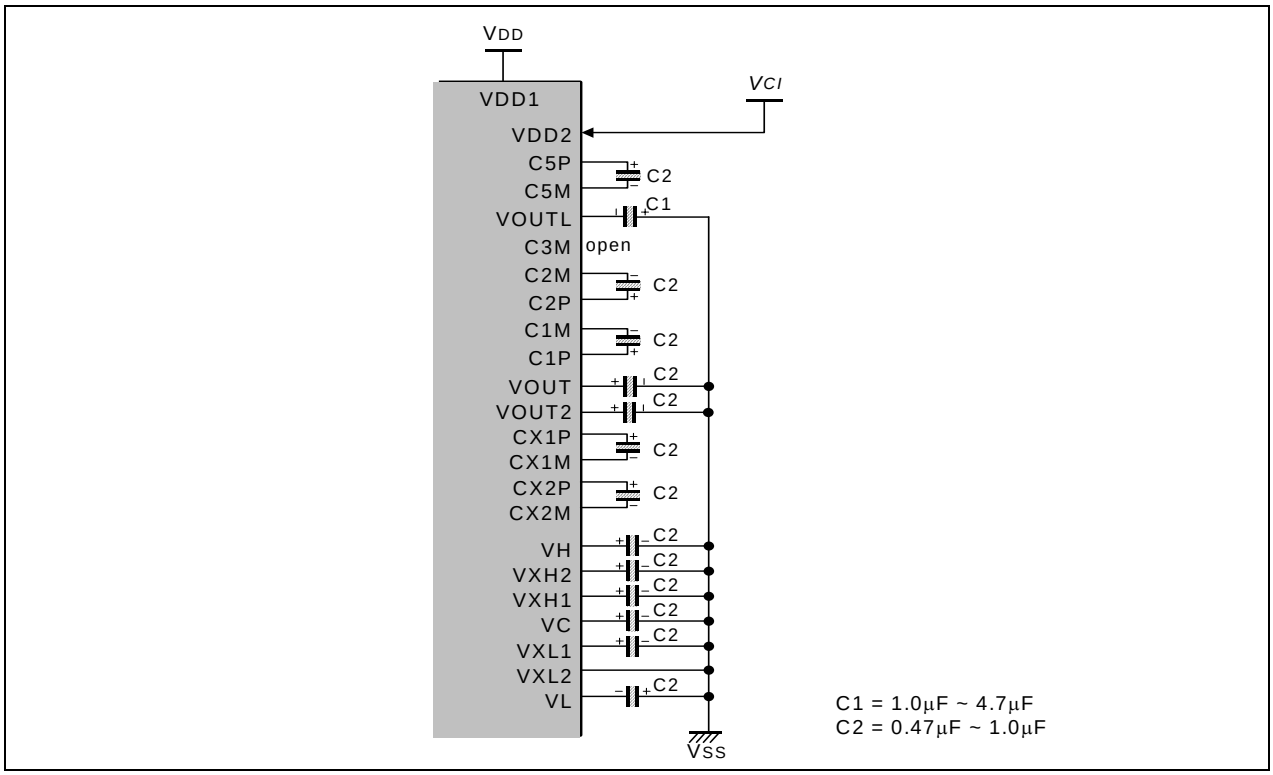


Fig. 5.11.7 Power circuit application example

5.11.9 Temperature Compensation

5.11.9.1 Temperature Sensor

The LDS176 requires temperature compensation implemented as a look up table in ROM as shown in ***Table 5.11.3***. The temperature of the display module is sensed on chip and converted to a 7 bit digital value. Over the temperature range of –35 to +92°C, the digital output of the sensor has a nominal resolution of 1°C. The digital output of the temperature sensor can be read by using temperature read function (see TMPREAD command). The output of the temperature sensor can be calibrated as follows:

1. A reset is applied to the driver to trigger a temperature measurement.
2. Wait 200ms for temperature measurement to be completed.
3. At a known temperature the output value of the temperature sensor is read.
4. The temperature value read from the chip is compared with the expected value at the given temperature

The temperature sensor measures the temperature about every 10 seconds and the first temperature sensing happens about 250msec after oscillator on start operation (by SLPOUT command). While the temperature conversion is being made the "Busy" flag is set. The read temperature value is only valid when the busy flag is zero.

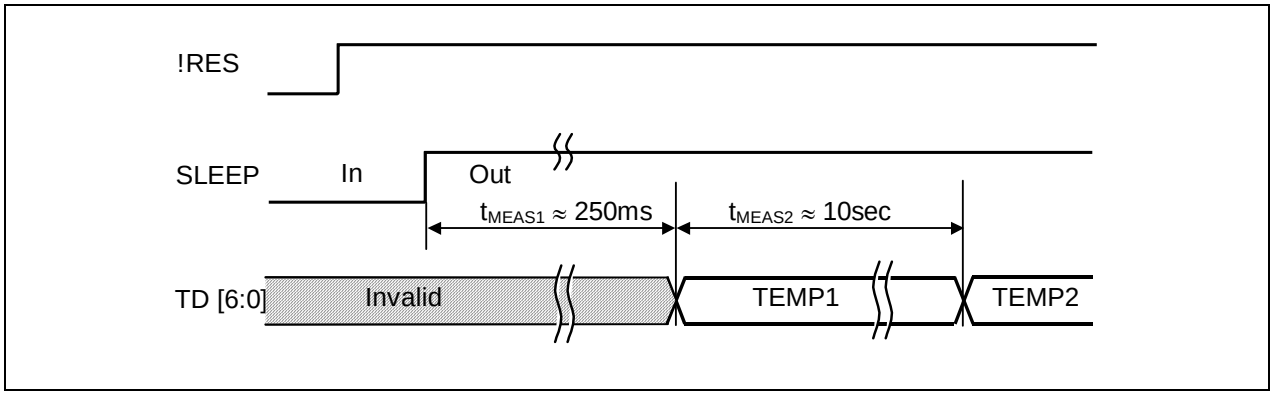


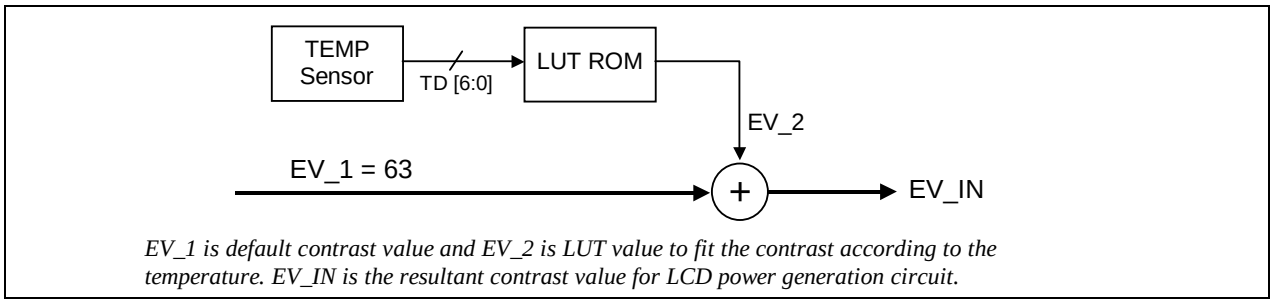
Fig. 5.11.8 Reset-Temperature Sense Timing

5.11.9.2 Contrast Adjustment

The 7-bit output of the temperature sensor (TD [6:0]) is used as an address for the look up table ROM. The ROM contains 128 7-bit words EV_2, which are used as a temperature dependent offset to make EV_IN for reference voltage.

LDS176 have two LUT ROM to support two different kinds liquid crystal panel, LUT can be selected by ID2 bit 4. If ID2 [4] = "0", the 1st LUT (R176_00) will be applied and if ID2 [4] = "1", the 2nd LUT (R176_01) will be applied for contrast adjustment according to the temperature.

Table 5.11.3 shows default ROM LUT output (EV_2) according to the temperature.



EV_1 is default contrast value and EV_2 is LUT value to fit the contrast according to the temperature. EV_IN is the resultant contrast value for LCD power generation circuit.

Fig. 5.11.9 Internal Contrast Adjustment Circuit

Table 5.11.3 ROM Look-up-Table Data (R176_00) : for Kyocera Panel (RR=4)

TD [6:0]	EV_2	TEMP	TD [6:0]	EV_2	TEMP	TD [6:0]	EV_2	TEMP	TD [6:0]	EV_2	TEMP
0	-28	-35	32	-14	-3	64	4	29	96	24	61
1	-28	-34	33	-14	-2	65	4	30	97	22	62
2	-28	-33	34	-14	-1	66	6	31	98	24	63
3	-26	-32	35	-12	0	67	8	32	99	24	64
4	-26	-31	36	-12	1	68	8	33	100	26	65
5	-28	-30	37	-12	2	69	8	34	101	26	66
6	-28	-29	38	-10	3	70	8	35	102	28	67
7	-26	-28	39	-10	4	71	10	36	103	28	68
8	-26	-27	40	-10	5	72	10	37	104	28	69
9	-26	-26	41	-10	6	73	12	38	105	30	70
10	-26	-25	42	-8	7	74	12	39	106	30	71
11	-24	-24	43	-8	8	75	14	40	107	28	72
12	-24	-23	44	-8	9	76	14	41	108	28	73
13	-24	-22	45	-6	10	77	14	42	109	28	74
14	-24	-21	46	-6	11	78	16	43	110	30	75
15	-22	-20	47	-6	12	79	16	44	111	28	76
16	-22	-19	48	-6	13	80	16	45	112	28	77
17	-24	-18	49	-4	14	81	16	46	113	28	78
18	-22	-17	50	-4	15	82	18	47	114	28	79
19	-22	-16	51	-4	16	83	18	48	115	28	80
20	-22	-15	52	-4	17	84	18	49	116	28	81
21	-20	-14	53	-4	18	85	18	50	117	30	82
22	-20	-13	54	0	19	86	20	51	118	30	83
23	-20	-12	55	0	20	87	20	52	119	28	84
24	-18	-11	56	0	21	88	20	53	120	28	85
25	-18	-10	57	0	22	89	20	54	121	28	86
26	-18	-9	58	2	23	90	22	55	122	28	87
27	-16	-8	59	2	24	91	22	56	123	28	88
28	-16	-7	60	4	25	92	22	57	124	28	89
29	-16	-6	61	4	26	93	22	58	125	28	90
30	-16	-5	62	4	27	94	24	59	126	28	91
31	-14	-4	63	4	28	95	24	60	127	26	92

Table 5.11.4 ROM Look-up-Table Data (R176_01) : for CTZ Panel (RR=5)

TD [6:0]	EV_2	TEMP	TD [6:0]	EV_2	TEMP	TD [6:0]	EV_2	TEMP	TD [6:0]	EV_2	TEMP
0	63	-35	32	22	-3	64	26	29	96	30	61
1	63	-34	33	20	-2	65	26	30	97	30	62
2	63	-33	34	20	-1	66	26	31	98	30	63
3	60	-32	35	20	0	67	26	32	99	30	64
4	56	-31	36	20	1	68	28	33	100	30	65
5	52	-30	37	20	2	69	28	34	101	30	66
6	48	-29	38	20	3	70	28	35	102	30	67
7	44	-28	39	20	4	71	28	36	103	30	68
8	40	-27	40	20	5	72	28	37	104	30	69
9	36	-26	41	20	6	73	28	38	105	30	70
10	34	-25	42	20	7	74	28	39	106	30	71
11	32	-24	43	20	8	75	30	40	107	28	72
12	30	-23	44	20	9	76	30	41	108	28	73
13	28	-22	45	20	10	77	30	42	109	26	74
14	26	-21	46	20	11	78	30	43	110	24	75
15	26	-20	47	20	12	79	30	44	111	24	76
16	26	-19	48	20	13	80	30	45	112	22	77
17	24	-18	49	20	14	81	32	46	113	20	78
18	24	-17	50	22	15	82	32	47	114	20	79
19	24	-16	51	22	16	83	32	48	115	18	80
20	24	-15	52	22	17	84	32	49	116	18	81
21	24	-14	53	22	18	85	32	50	117	16	82
22	24	-13	54	22	19	86	32	51	118	14	83
23	24	-12	55	22	20	87	32	52	119	12	84
24	24	-11	56	24	21	88	32	53	120	10	85
25	24	-10	57	24	22	89	30	54	121	10	86
26	24	-9	58	24	23	90	30	55	122	8	87
27	22	-8	59	26	24	91	30	56	123	6	88
28	22	-7	60	26	25	92	30	57	124	4	89
29	22	-6	61	26	26	93	30	58	125	4	90
30	22	-5	62	26	27	94	30	59	126	2	91
31	22	-4	63	26	28	95	30	60	127	2	92

5.11.9.3 Frame Frequency Adjustment

The 7-bit output of the temperature sensor (TD [6:0]) is also used for an automatic frequency adjustment circuit. When the read temperature is decreasing state, the frame frequency is adjusted as the temperature crosses the preset boundary values, TA, TB, and TC as shown below. When the read temperature is increasing state, the frame frequency is adjusted at the preset boundary values + TH in order to avoid unstable display when the measured temperature changes around a preset boundary value.

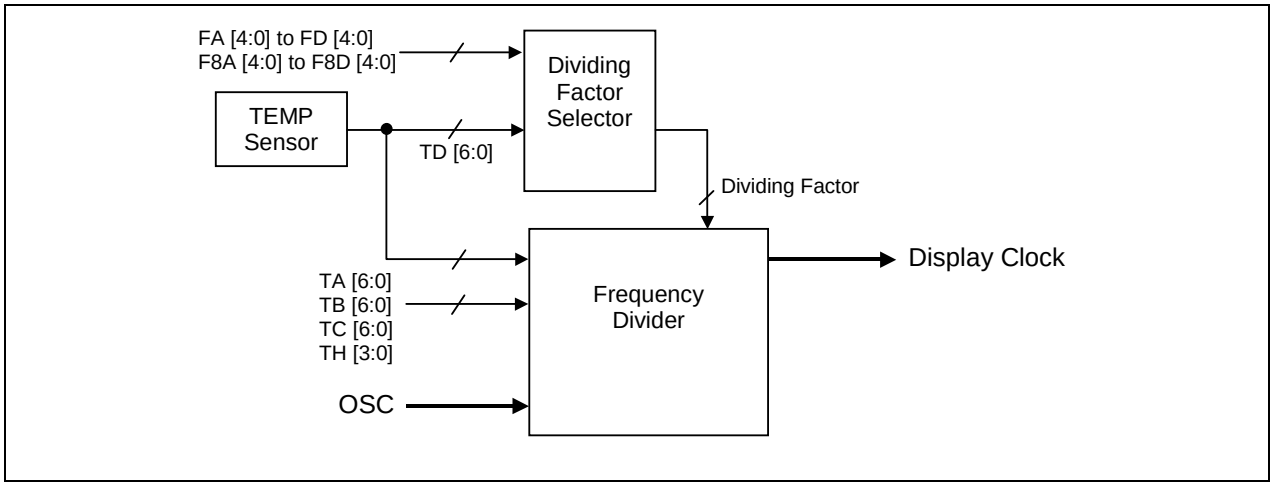


Fig. 5.11.10 Frame Frequency Adjustment Circuit

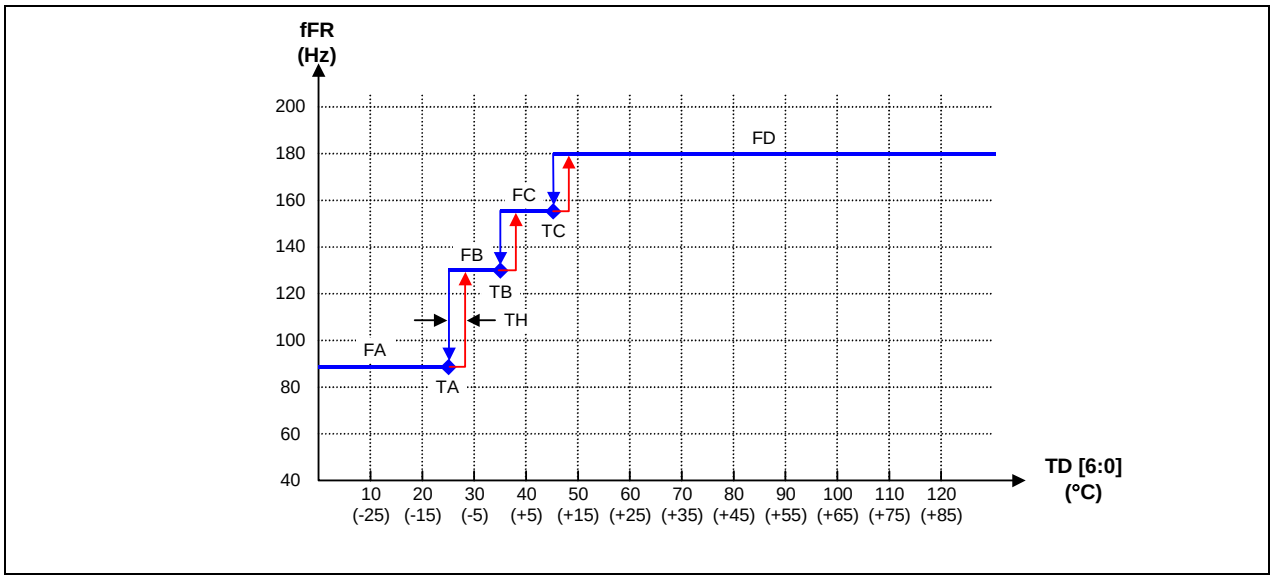


Fig. 5.11.11 Default Frame Frequency Adjustment Chart

5.12 POWER ON/OFF SEQUENCE

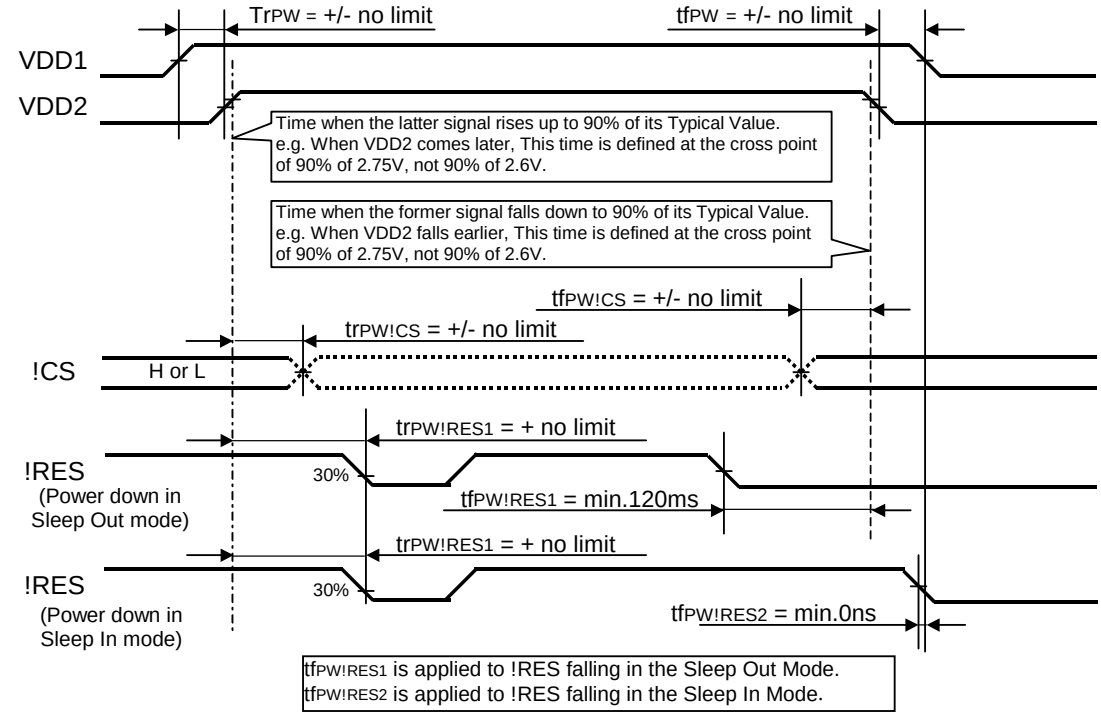
VDD1 and VDD2 can be applied in any order.
VDD2 and VDD1 can be powered down in any order.
During power off, if LCD is in the Sleep Out mode, VDD2 and VDD1 must be powered down minimum 120msec after !RES has been released.
During power off, if LCD is in the Sleep In mode, VDD1 or VDD2 can be powered down minimum 0msec after !RES has been released.
!SCE can be applied at any timing or can be permanently grounded. !RES has priority over !SCE.

There will be no damage to the display module if the power sequences are not met.
There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
If !RES line is not held stable by host during Power On Sequence as defined in Sections 5.12.1 and 5.12.2, then it will be necessary to apply a Hardware Reset (!RES) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

5.12.1 Case 1 – !RES line is held High or Unstable by Host at Power On

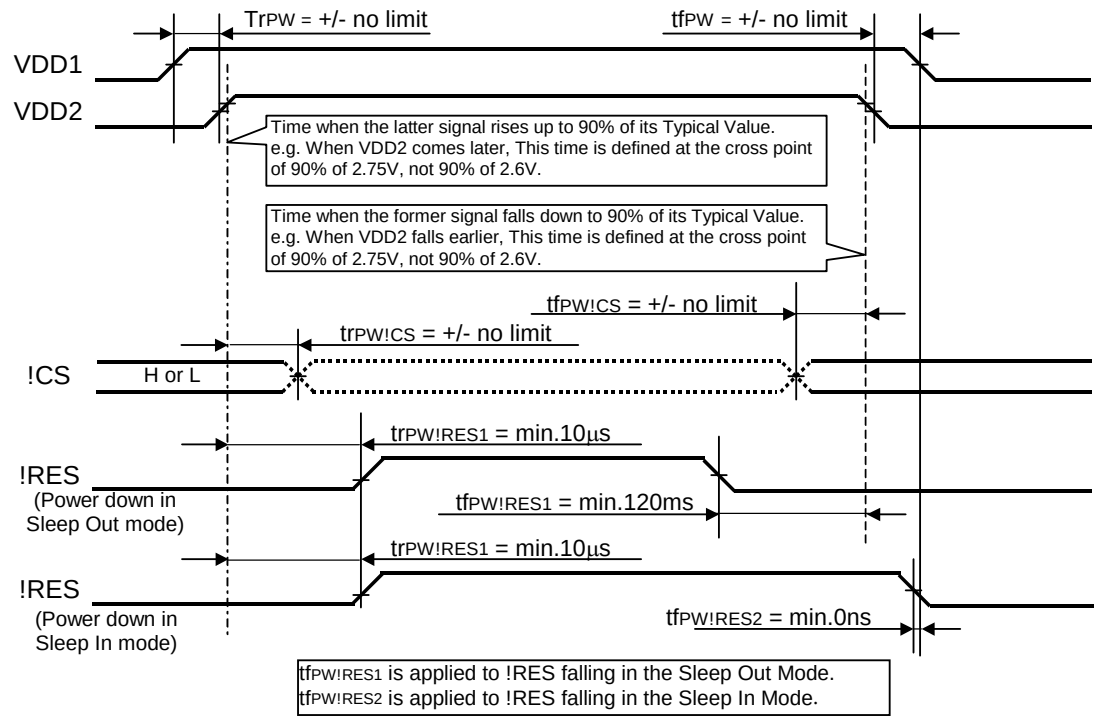
If !RES line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD2 and VDD1 have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

5.12.2 Case 2 – !RES line is held Low by host at Power On

If !RES line is held Low (and stable) by the host during Power On, then the !RES must be held low for minimum 10µsec after both VDD2 and VDD1 have been applied.

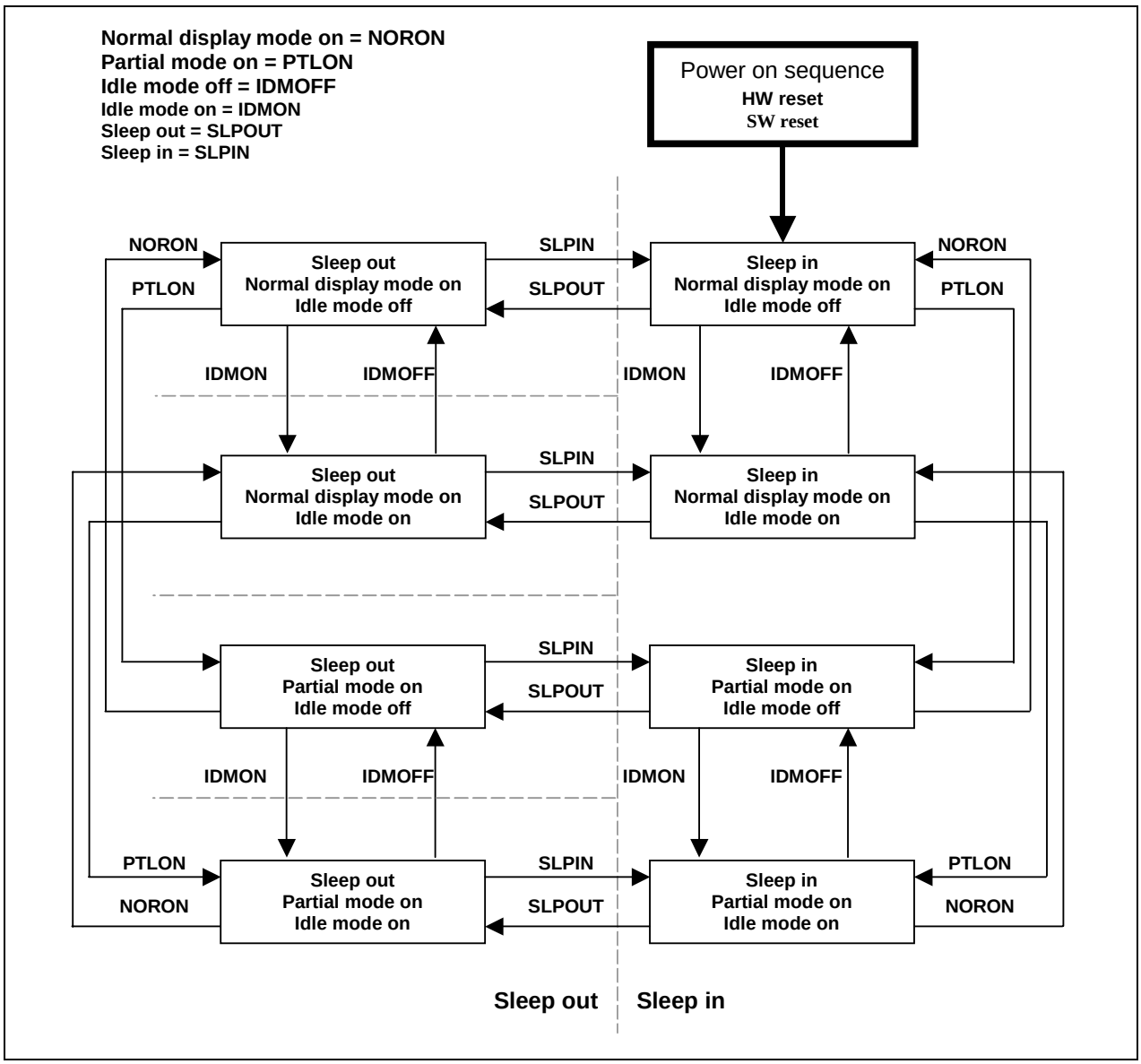


Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

5.13 UNCONTROLLED POWER OFF

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects on the display.

5.14 POWER FLOW CHART FOR DIFFERENT POWER MODES



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

2: There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode.

6 INSTRUCTION DESCRIPTION

6.1 INSTRUCTION CODE 0 (ISS=0, MESSI-8)

6.1.1 Instruction Code Table

Table 6.1.1 Instruction Code0 (ISS=0)

"-": Don't care

Instruction	Refer	ISS	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)	Function
NOP	6.1.2	0	0	↑	1	0	0	0	0	0	0	0	0	**(00h)**	No Operation
SWRESET	6.1.3	0	0	↑	1	0	0	0	0	0	0	0	1	**(01h)**	Software reset
BSTROFF	6.1.4	0	0	↑	1	0	0	0	0	0	0	1	0	**(02h)**	Booster off (only for test purpose)
BSTRON	6.1.5	0	0	↑	1	0	0	0	0	0	0	1	1	**(03h)**	Booster on (only for test purpose)
RDDID	6.1.6	0	0	↑	1	0	0	0	0	0	1	0	0	**(04h)**	Read Display ID
		0	1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read
		0	1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-	ID1 read
		0	1	1	↑	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-	ID2 read
		0	1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-	ID3 read
RDDST	6.1.7	0	0	↑	1	0	0	0	0	1	0	0	1	**(09h)**	Read Display Status
		0	1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read
		0	1	1	↑	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	-	-
		0	1	1	↑	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	-	-
		0	1	1	↑	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	-	-
		0	1	1	↑	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	-	-
SLPIN	6.1.8	0	0	↑	1	0	0	0	1	0	0	0	0	**(10h)**	Sleep in & booster off
SLPOUT	6.1.9	0	0	↑	1	0	0	0	1	0	0	0	1	**(11h)**	Sleep out & booster on
PTLON	6.1.10	0	0	↑	1	0	0	0	1	0	0	1	0	**(12h)**	Partial mode on
NORON	6.1.11	0	0	↑	1	0	0	0	1	0	0	1	1	**(13h)**	Partial off (Normal)
INVOFF	6.1.12	0	0	↑	1	0	0	1	0	0	0	0	0	**(20h)**	Display inversion off (normal)
INVON	6.1.13	0	0	↑	1	0	0	1	0	0	0	0	1	**(21h)**	Display inversion on
APOFF	6.1.14	0	0	↑	1	0	0	1	0	0	0	1	0	**(22h)**	All pixel off (only for test purpose)
APON	6.1.15	0	0	↑	1	0	0	1	0	0	0	1	1	**(23h)**	All pixel on (only for test purpose)
WRCNTR		0	0	↑	1	0	0	1	0	0	1	0	1	**(25h)**	Write contrast
	6.1.16	0	1	↑	1	-	EV6	EV5	EV4	EV3	EV2	EV1	EV0	-	EV = 0 to 127
DISPOFF	6.1.17	0	0	↑	1	0	0	1	0	1	0	0	0	**(28h)**	Display off
DISPON	6.1.18	0	0	↑	1	0	0	1	0	1	0	0	1	**(29h)**	Display on
CASET		0	0	↑	1	0	0	1	0	1	0	1	0	**(2Ah)**	Column address set
	6.1.19	0	1	↑	1	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	-	X_ADR start: 0 ≤ XS ≤ 83h
		0	1	↑	1	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	-	X_ADR end: XS ≤ XE ≤ 83h
RASET		0	0	↑	1	0	0	1	0	1	0	1	1	**(2Bh)**	Row address set
	6.1.20	0	1	↑	1	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	-	Y_ADR start: 0 ≤ YS ≤ 83h
		0	1	↑	1	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	-	Y_ADR end: YS ≤ YE ≤ 83h
RAMWR		0	0	↑	1	0	0	1	0	1	1	0	0	**(2Ch)**	Memory write
	6.1.21	0	1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	-	Write data
RAMRD	6.1.22	0	0	↑	1	0	0	1	0	1	1	1	0	**(2Eh)**	Memory read
		0	1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read
		0	1	1	↑	D7	D6	D5	D4	D3	D2	D1	D0	-	Read data

Table 6.1.2 Instruction Code0 (ISS=0 Continued)

"-": Don't care

Instruction	Refer	ISS	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)	Function
RGBSET	6.1.23	0	0	↑	1	0	0	1	0	1	1	0	1	**(2Dh)**	Color set for 256 color display
		0	1	↑	1	-	-	-	-	R3	R2	R1	R0	-	Red tone (000)
		0	1	↑	1	:	:	:	:	:	:	:	:	:	: -
		0	1	↑	1	-	-	-	-	R3	R2	R1	R0	-	Red tone (111)
		0	1	↑	1	-	-	-	-	G3	G2	G1	G0	-	Green tone (000)
		0	1	↑	1	:	:	:	:	:	:	:	:	:	: -
		0	1	↑	1	-	-	-	-	G3	G2	G1	G0	-	Green tone (111)
		0	1	↑	1	-	-	-	-	B3	B2	B1	B0	-	Blue tone (00)
		0	1	↑	1	:	:	:	:	:	:	:	:	:	: -
		0	1	↑	1	-	-	-	-	B3	B2	B1	B0	-	Blue tone (11)
PTLAR	6.1.24	0	0	↑	1	0	0	1	1	0	0	0	0	**(30h)**	Partial start/end address set
		0	1	↑	1	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-	Start address (0,1,2, …, 131)
		0	1	↑	1	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	-	End address (0,1,2, …, 131)
SCRLAR	6.1.25	0	0	↑	1	0	0	1	1	0	0	1	1	**(33h)**	Scroll area set (2-line unit)
		0	1	↑	1	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-	TFA = 0,1,2, … , 132
		0	1	↑	1	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	-	VSA = 0,1,2, … , 132
		0	1	↑	1	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	-	BFA = 0,1,2, … , 132
TEOFF	6.1.26	0	0	↑	1	0	0	1	1	0	1	0	0	**(34h)**	Tearing effect line off
TEON	6.1.27	0	0	↑	1	0	0	1	1	0	1	0	1	**(35h)**	Tearing effect mode set & on
		0	1	↑	1	-	-	-	-	-	-	-	M	-	"0": mode1, "1": mode2
MADCTR	6.1.28	0	0	↑	1	0	0	1	1	0	1	1	0	**(36h)**	Memory data access control
		0	1	↑	1	MY	MX	MV	ML	RGB	-	-	-	-	-
VSCSAD	6.1.29	0	0	↑	1	0	0	1	1	0	1	1	1	**(37h)**	Scroll start address of RAM
		0	1	↑	1	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	-	SSA = 0, 1, 2, … , 131
IDMOFF	6.1.30	0	0	↑	1	0	0	1	1	1	0	0	0	**(38h)**	Idle mode off
IDMON	6.1.31	0	0	↑	1	0	0	1	1	1	0	0	1	**(39h)**	Idle mode on
COLMOD	6.1.32	0	0	↑	1	0	0	1	1	1	0	1	0	**(3Ah)**	Interface pixel format
		0	1	↑	1	-	-	-	-	-	P2	P1	P0	-	Interface format
RDID1	6.1.33	0	0	↑	1	1	1	0	1	1	0	1	0	**(DAh)**	Read ID1
		0	1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read
		0	1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-	Read parameter
RDID2	6.1.34	0	0	↑	1	1	1	0	1	1	0	1	1	**(DBh)**	Read ID2
		0	1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read
		0	1	1	↑	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-	Read parameter
RDID3	6.1.35	0	0	↑	1	1	1	0	1	1	1	0	0	**(DCh)**	Read ID3
		0	1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read
		0	1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-	Read parameter

Table 6.1.3 Instruction Code0 (ISS=0 Extended code set, EXTB=0)

"-": Don't care

Instruction	Refer	ISS	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)	Function
CLKINT	6.1.36	0	0	↑	1	1	0	1	1	0	0	0	0	**(B0h)**	Internal oscillator select
CLKEXT	6.1.37	0	0	↑	1	1	0	1	1	0	0	0	1	**(B1h)**	External oscillator select
FRMSEL	6.1.38	0	0	↑	1	1	0	1	1	0	1	0	0	**(B4h)**	Frame frequency select
		0	1	↑	1	-	-	-	FA4	FA3	FA2	FA1	FA0	-	Frame frequency in Temp range A
		0	1	↑	1	-	-	-	FB4	FB3	FB2	FB1	FB0	-	Frame frequency in Temp range B
		0	1	↑	1	-	-	-	FC4	FC3	FC2	FC1	FC0	-	Frame frequency in Temp range C
		0	1	↑	1	-	-	-	FD4	FD3	FD2	FD1	FD0	-	Frame frequency in Temp range D
FRM8SEL	6.1.39	0	0	↑	1	1	0	1	1	0	1	0	1	**(B5h)**	Frame frequency select (8-color)
		0	1	↑	1	-	-	-	F8A4	F8A3	F8A2	F8A1	F8A0	-	Frame frequency in Temp range A
		0	1	↑	1	-	-	-	F8B4	F8B3	F8B2	F8B1	F8B0	-	Frame frequency in Temp range B
		0	1	↑	1	-	-	-	F8C4	F8C3	F8C2	F8C1	F8C0	-	Frame frequency in Temp range C
		0	1	↑	1	-	-	-	F8D4	F8D3	F8D2	F8D1	F8D0	-	Frame frequency in Temp range D
TMPRNG	6.1.40	0	0	↑	1	1	0	1	1	0	1	1	0	**(B6h)**	Temp range set
		0	1	↑	1	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	-	Temp range A
		0	1	↑	1	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	-	Temp range B
		0	1	↑	1	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	-	Temp range C
TMPHIS	6.1.41	0	0	↑	1	1	0	1	1	0	1	1	1	**(B7h)**	Temp hysteresis range set
		0	1	↑	1	-	-	-	-	TH3	TH2	TH1	TH0	-	Hysteresis value set
TMPREAD	6.1.42	0	0	↑	1	1	0	1	1	1	0	0	0	**(B8h)**	Temperature read back
		0	1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read
		0	1	1	↑	BF	T6	T5	T4	T3	T2	T1	T0	-	Read parameter
DISCTR	6.1.43	0	0	↑	1	1	0	1	1	1	0	1	0	**(BAh)**	Display control
		0	1	↑	1	-	-	-	-	-	FS2	FS1	FS0	-	F1/F2 pattern
		0	1	↑	1	-	-	-	FINV	NL3	NL2	NL1	NL0	-	FR inversion-set value
EPVOL	6.1.44	0	0	↑	1	1	0	1	1	1	0	1	1	**(BBh)**	Electronic volume offset
		0	1	↑	1	-	-	EOF5	EOF4	EOF3	EOF2	EOF1	EOF0	-	EV offset
		0	1	↑	1	-	-	-	-	-	-	-	-	-	Dummy
		0	1	↑	1	-	-	-	-	-	ROF2	ROF1	ROF0	-	RR offset
EPWRIN	6.1.45	0	0	↑	1	1	1	0	1	0	0	0	1	**(D1h)**	EEPROM write start
EPWROUT	6.1.46	0	0	↑	1	1	1	0	1	0	0	0	0	**(D0h)**	EEPROM write end
RDEV	6.1.47	0	0	↑	1	1	1	0	1	0	1	0	0	**(D4h)**	Read internal contrast (EV_IN)
		0	1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read
		0	1	1	↑	-	EV6	EV5	EV4	EV3	EV2	EV1	EV0	-	Read parameter
RDRR	6.1.48	0	0	↑	1	1	1	0	1	0	1	0	1	**(D5h)**	Read internal resistor ratio (RR_IN)
		0	1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read
		0	1	1	↑	-	-	-	-	-	RR2	RR1	RR0	-	Read parameter
TEST1	6.1.49	0	0	↑	1	1	1	1	0	-	-	-	-	**(E-h)**	Test command1.
TEST2	6.1.50	0	0	↑	1	1	1	1	1	-	-	-	-	**(F-h)**	Test command2.

NOTE:

1) After the H/W reset by !RES pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section)

2) To use extended code set, EXTB should be connected to VSS. Normally, expended code set is just used for module test. If extended code is not enabled all the extended code set will be ignored and regarded as NOP (00h) command.

3) Undefined commands are treated as NOP (00 h) command.

4) Commands 10h, 12h, 13h, 20h, 21h, 25h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h) of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

6.1.2 NOP (00h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
00	NOP	0	↑	1	0	0	0	0	0	0	0	0	(00h)
00	Parameter	No Parameter											

Description	This command is empty command. It does not have effect on the display module. However it can be used to terminate RAM data write or read as described in RAMWR (Memory Write), RAMRD (Memory Read) and parameter write commands.
Restriction	-
Register Availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status: Default Value Power On Sequence: N/A S/W Reset: N/A H/W Reset: N/A
Flow Chart	-

6.1.3 SWRESET: Software Reset (01h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	SWRESET	0	↑	1	0	0	0	0	0	0	0	1	(01h)
0	Parameter	No Parameter											

Description

When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all segment & common outputs are set to VC (display off: blank display). (See default tables in each command description)

Note: The Frame Memory contents are not affected by this command.

Restriction

It will be necessary to wait 5msec before sending new command following software reset

The display module loads all display supplier's factory default values to the registers during this 5ms.

If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command.

Software Reset command cannot be sent during Sleep Out sequence.

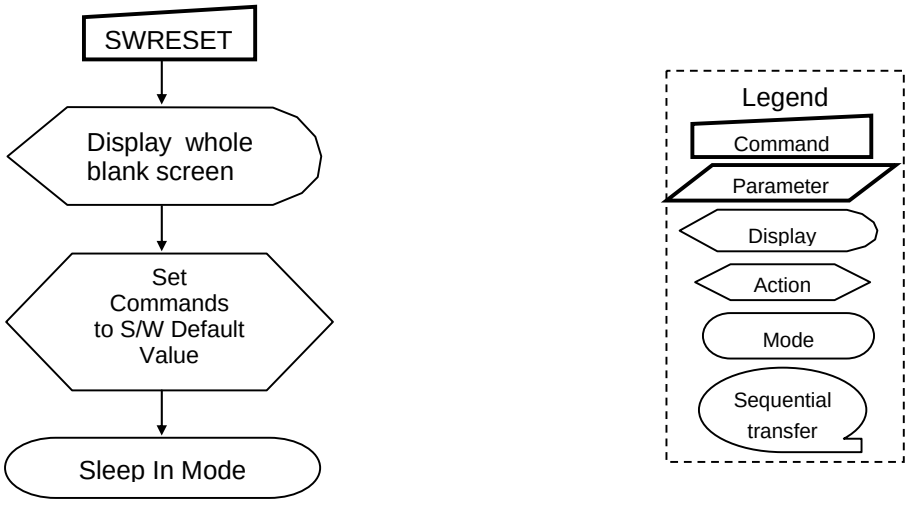
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart

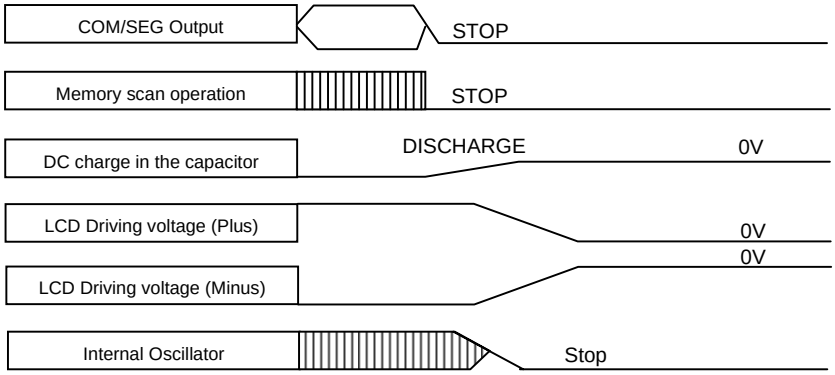


6.1.4 BSTROFF: Booster Off (02h) (Only for Test Purposes)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	BSTROFF	0	↑	1	0	0	0	0	0	0	1	0	(02h)
0	Parameter	No Parameter											

Description

This command turns off booster related circuit (Oscillator and DC/DC Converter) and panel scanning is stopped.



MCU interface and memory are still working and the memory keeps its contents

It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilise, but to discharge all the capacitor value to ground, it will take about 120msec.

Restriction

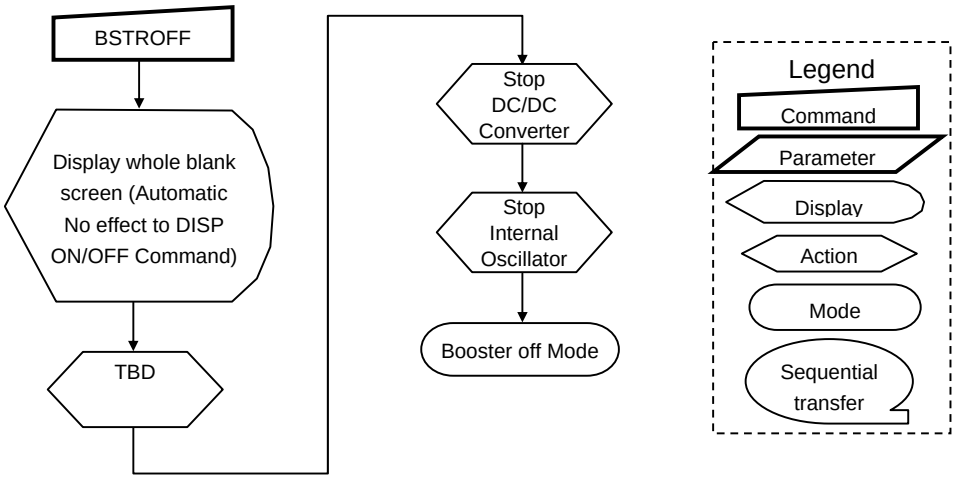
This command has no effect when module is already in Booster Off mode. Booster Off Mode can be exit by the Booster On Command (03h) or Sleep Out Command (11h).

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Booster off mode
S/W Reset	Booster off mode
H/W Reset	Booster off mode

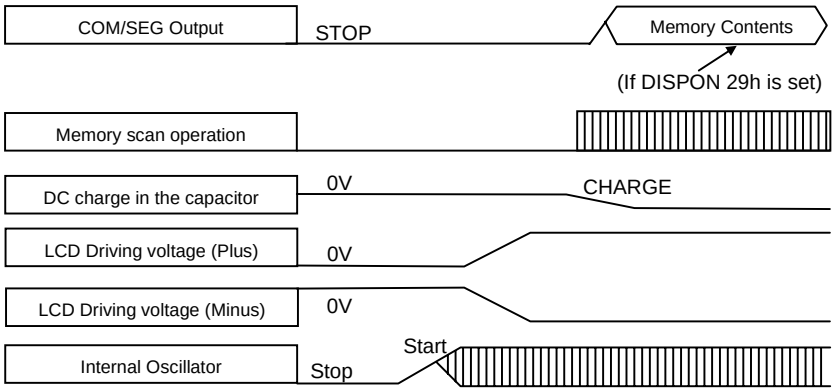
Flow Chart	It takes more than 120msec to get into Booster Off mode after BSTROFF command issued. The results of booster off can be checked by RDDST (09h) command Bit31. 

6.1.5 BSTRON: Booster ON (03h) (Only for Test Purposes)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	BSTRON	0	↑	1	0	0	0	0	0	0	1	1	(03h)
0	Parameter	No Parameter											

Description

This command turns on booster related circuit (Oscillator and DC/DC converter) and panel scanning is started.



Restriction

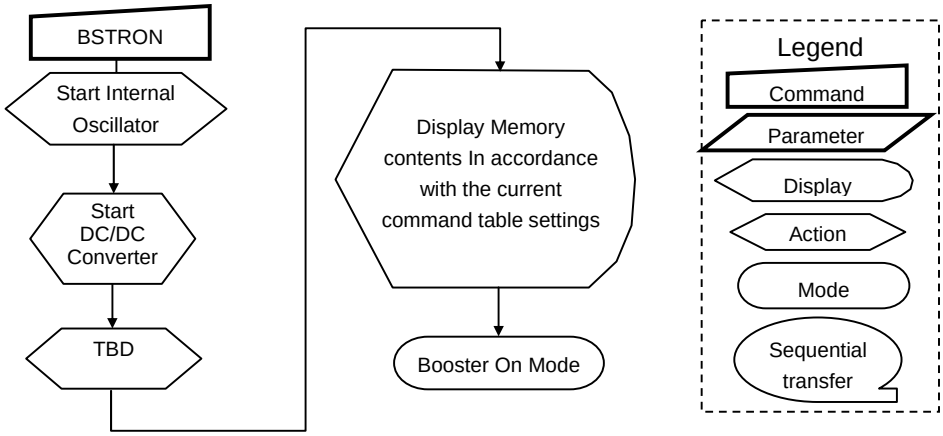
This command has no effect when module is already in Booster On mode. Booster On Mode can be exit by the Booster Off Command (02h) or Sleep In Command (10h).
It will be necessary to wait 120msec for the supply voltages and clock circuits to stabilize.
During 120msec after BSTRON command, display on register will be blocked to “L” (off).

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Booster off mode
S/W Reset	Booster off mode
H/W Reset	Booster off mode

Flow Chart	It takes 120msec to get into Booster On mode after BSTRON command issued. The results of booster on can be checked by RDDST (09h) command Bit31. 

6.1.6 RDDID: Read Display ID (04h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	RDDID	0	↑	1	0	0	0	0	0	1	0	0	(04h)
0	Dummy Read	1	1	↑	-	-	-	-	-	-	-	-	-
0	2nd parameter	1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
0	3rd parameter	1	1	↑	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
0	4th parameter	1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

Description

This read byte returns 24-bit display identification information.

The 1st parameter is dummy data

The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.

The 3rd parameter (ID26 to ID20): LCD module/driver version ID

The 4th parameter (ID37 to UD30): LCD module/driver ID.

NOTE: Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.

Restriction

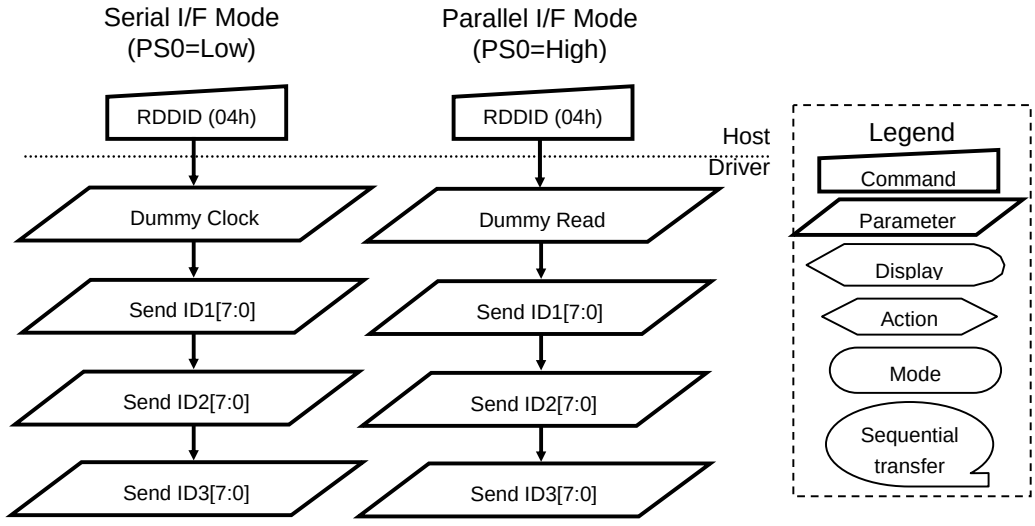
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ID1	ID2 (binary)	ID3
Power On Sequence	45h	80 ~ FFh (Not Fixed)	03h
S/W Reset	45h	80 ~ FFh (Not Fixed)	03h
H/W Reset	45h	80 ~ FFh (Not Fixed)	03h

Flow Chart



6.1.7 RDDST: Read Display Status (09h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	RDDST	0	↑	1	0	0	0	0	1	0	0	1	(09h)
0	Dummy Read	1	1	↑	-	-	-	-	-	-	-	-	-
0	2nd parameter	1	1	↑	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	-
0	3rd parameter	1	1	↑	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	-
0	4th parameter	1	1	↑	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	-
0	5th parameter	1	1	↑	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
ST31	Booster Voltage Status	"1"=Booster on, "0"=off
ST30	Row Address Order	"1"=Decrement, "0"=Increment
ST29	Column Address Order	"1"=Decrement, "0"=Increment
ST28	Row/Column Order (MV)	"1"= Row/column exchange (MV=1) "0"= Normal (MV=0)
ST27	Scan Address Order	"1"=Decrement, "0"=Increment
ST26	RGB/BGR Order	"1"=BGR, "0"=RGB
ST25	Not Used	"0"
ST24	Not Used	"0"
ST23	Not Used	"0"
ST22 ST21 ST20	Interface Colour Pixel Format Definition	"010" = 8-bit / pixel, "011" = 12-bit / pixel type A "101" = 16-bit / pixel, "110" = 12-bit / pixel type B
ST19	Idle Mode On/Off	"1" = On, "0" = Off
ST18	Partial Mode On/Off	"1" = On, "0" = Off
ST17	Sleep In/Out	"1" = In, "0" = Out
ST16	Display Normal Mode On/Off	"1" = Partial Display, "0" = Normal Display
ST15	Vertical Scrolling Status	"1" = Scroll on, "0" = Scroll off
ST14	Not Used	"0"
ST13	Inversion Status	"1" = On, "0" = Off
ST12	All Pixels On	"1" = mode On, "0" = mode Off
ST11	All Pixels Off	"1" = mode On, "0" = mode Off
ST10	Display On/Off	"1" = On, "0" = Off
ST9	Tearing Effect Line On/Off	"1" = On, "0" = Off
ST8	Not Used	"0"
ST7	Not Used	"0"
ST6	Not Used	"0"
ST5	Tearing effect line mode	"0" = mode1, "1" = mode2
ST4	Not Used	"0"
ST3	Not Used	"0"
ST2	Not Used	"0"
ST1	Not Used	"0"
ST0	Not Used	"0"

Restriction

Register Availability

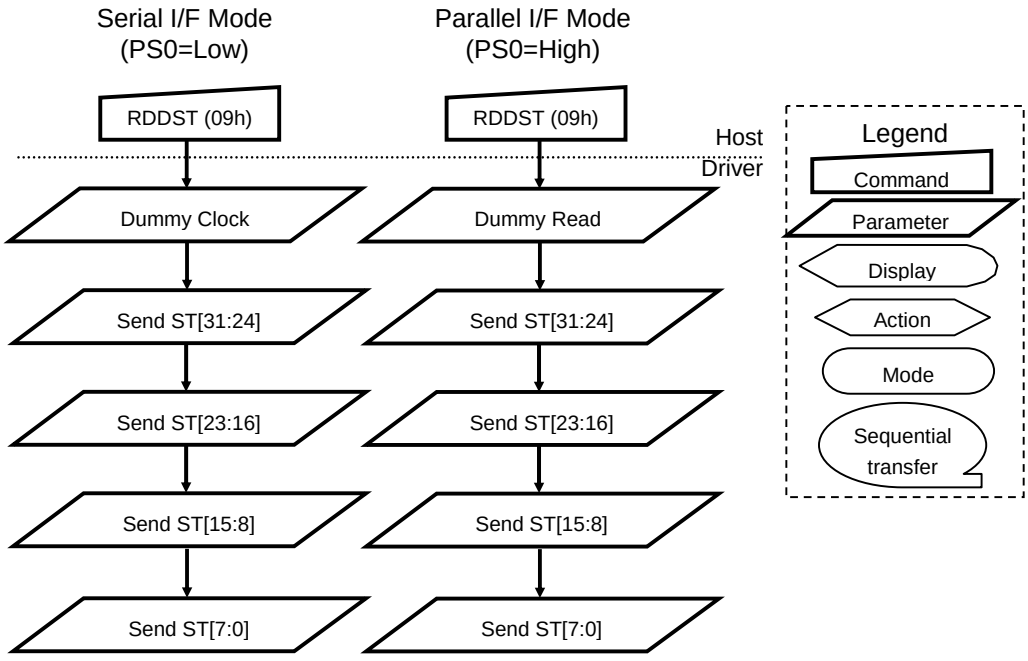
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000 0000_0011 0010_0000 0000_0000 0000
S/W Reset	0XXX XX00_0XXX 0010_0000 0000_0000 0000
H/W Reset	0000 0000_0011 0010_0000 0000_0000 0000

"XXX": No Change

Flow Chart



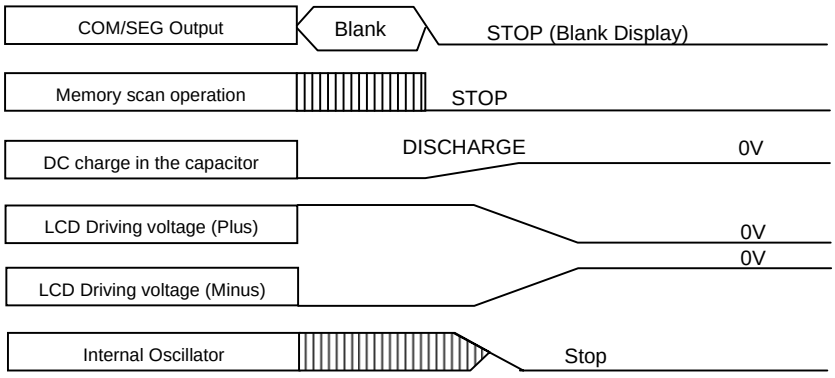
6.1.8 SLPIN: Sleep In (10h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	SLPIN	0	↑	1	0	0	0	1	0	0	0	0	(10h)
0	Parameter	No Parameter											

Description

This command causes the LCD module to enter the minimum power consumption mode.

In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.



MCU interface and memory are still working and the memory keeps its contents

Restriction

This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).

It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.

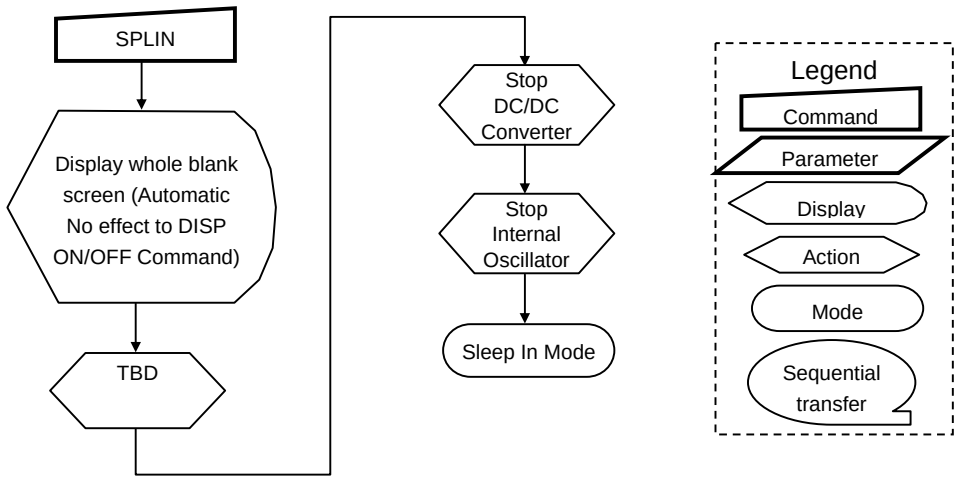
It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart	It takes 120 msec to get into Sleep In mode (booster off state) after SLPIN command issued. The results of booster off can be checked by RDDST (09h) command Bit31. 

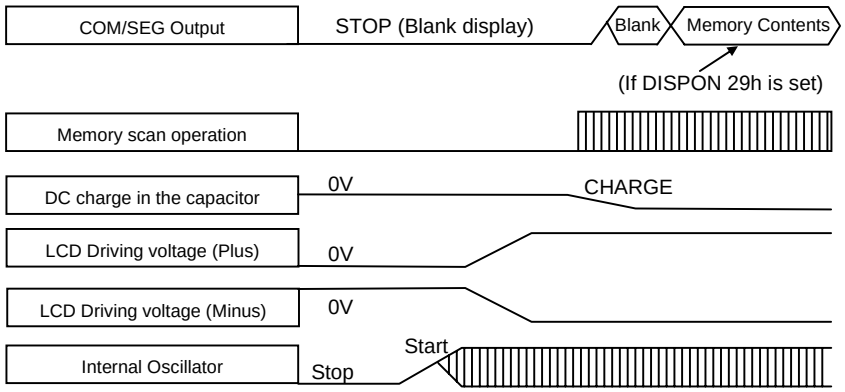
6.1.9 SLPOUT: Sleep Out (11h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	SLPOUT	0	↑	1	0	0	0	1	0	0	0	1	(11h)
0	Parameter	No Parameter											

Description

This command turns off sleep mode.

In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.



Restriction

This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h).

It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.

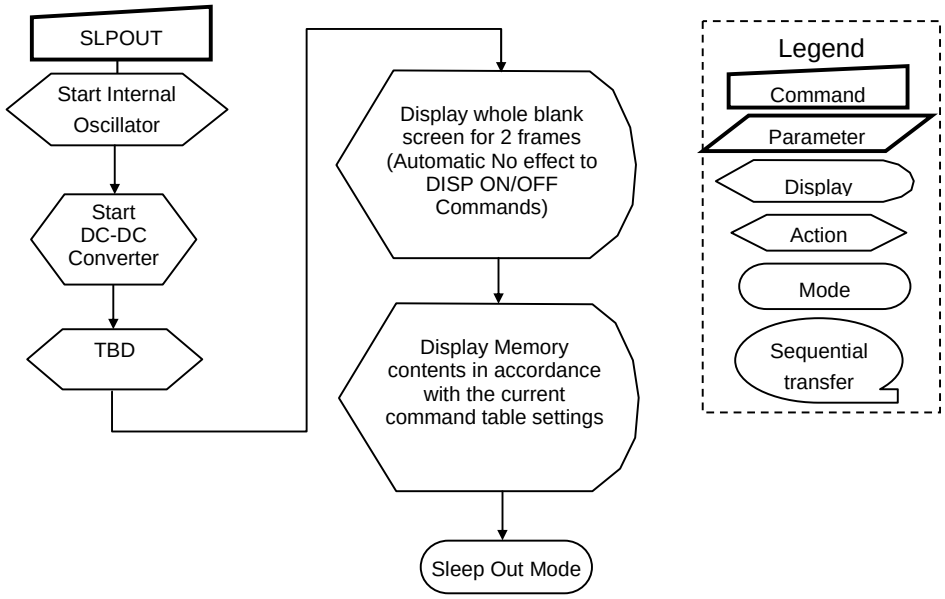
It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart	It takes 120msec to become Sleep Out mode (booster on mode) after SLPOUT command issued. The results of booster on can be checked by RDDST (09h) command Bit31. 

6.1.10 PTLON: Partial Display Mode On (12h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	PTLON	0	↑	1	0	0	0	1	0	0	1	0	(12h)
0	Parameter	No Parameter											

Description	This command turns on Partial mode. The partial mode window is described by the Partial Area command (30_H) Exit from PTLON by Normal Display Mode On command (13_H) There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.
Restriction	This command has no effect when Partial mode is active.
Register Availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status: Default Value Power On Sequence: Partial mode off S/W Reset: Partial mode off H/W Reset: Partial mode off
Flow Chart	See Partial Area (30h)

6.1.11 NORON: Normal Display Mode On (13h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	NORON	0	↑	1	0	0	0	1	0	0	1	1	(13h)
0	Parameter	No Parameter											

Description	This command returns the display to normal mode. Normal display mode on means Partial mode off, Scroll mode Off. Exit from NORON by the Partial mode On command (12h) There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.
Restriction	This command has no effect when Normal Display mode is active.
Register Availability	Status / Availability: Normal Mode On, Idle Mode Off, Sleep Out — Yes Normal Mode On, Idle Mode On, Sleep Out — Yes Partial Mode On, Idle Mode Off, Sleep Out — Yes Partial Mode On, Idle Mode On, Sleep Out — Yes Sleep In — Yes
Default	Status / Default Value: Power On Sequence — Normal Mode On S/W Reset — Normal Mode On H/W Reset — Normal Mode On
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command

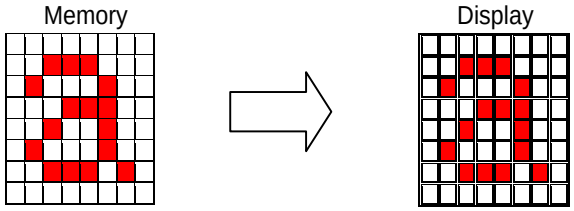
6.1.12 INVOFF: Display Inversion Off (20h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	INVOFF	0	↑	1	0	0	1	0	0	0	0	0	(20h)
0	Parameter	No parameter											

Description

This command is used to recover from display inversion mode.
This command makes no change of contents of frame memory.
This command does not change any other status.

(Example)



Restriction

This command has no effect when module is already inversion off mode.
NOTE: In case of normally black panel, resultant display after INVOFF and INVON will be exchanged.

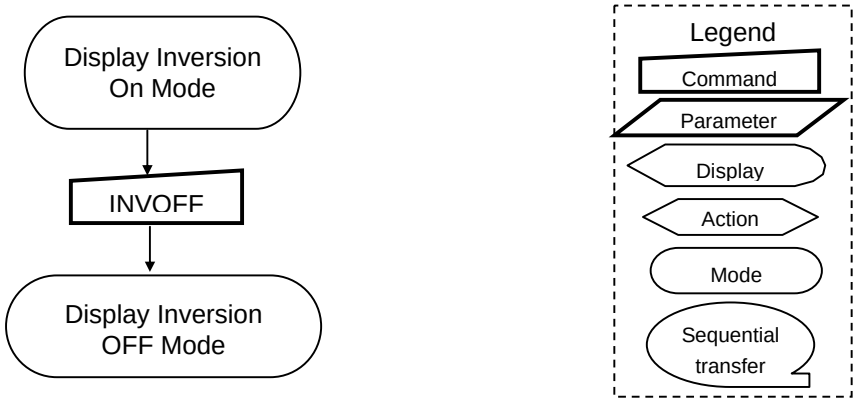
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



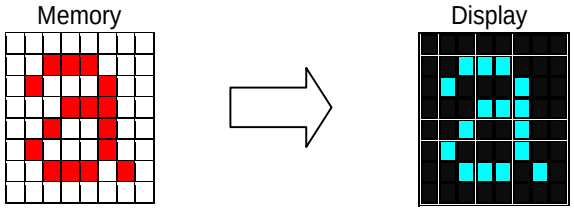
6.1.13 INVON: Display Inversion On (21h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	INVON	0	↑	1	0	0	1	0	0	0	0	1	(21h)
0	Parameter	No Parameter											

Description

This command is used to enter into display inversion mode
This command makes no change of contents of frame memory.
This command does not change any other status.
To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.

(Example)



Restriction

This command has no effect when module is already Inversion On mode.
NOTE: In case of normally black panel, resultant display after INVOFF and INVON will be exchanged.

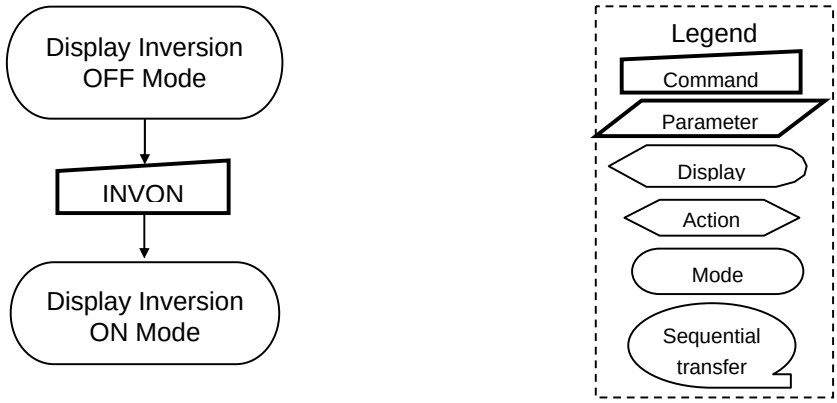
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



6.1.14 APOFF: All Pixels Off (22h) (Only for Test Purposes)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	APOFF	0	↑	1	0	0	1	0	0	0	1	0	(22h)
0	Parameter	No Parameter											

Description

This command is only used for test purpose e.g. pixel response time (on/off) measurements on the passive matrix display. Therefore, it is possible that this command is not used for final product software.

All driver outputs become “Low” data state and display becomes black.

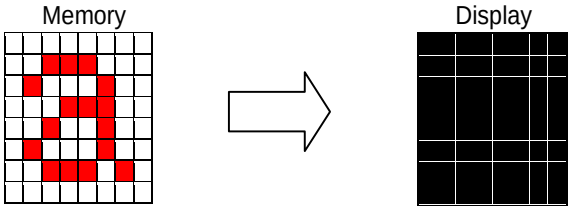
This command makes no change of contents of display memory.

This command does not change any other status.

Exit commands are “All Pixels On”, “Normal Display Mode On” and “Partial Display On”.

The display is showing the contents of the frame memory after “Normal Display Mode On” and “Partial Display On” commands.

(Example)



Restriction

This command has no effect when module is already All Pixel Off mode.

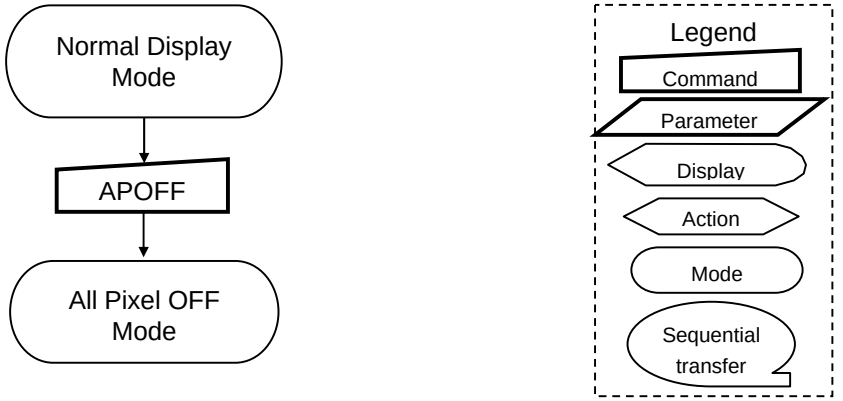
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All pixel off mode disable
S/W Reset	All pixel off mode disable
H/W Reset	All pixel off mode disable

Flow Chart



6.1.15 APON: All Pixels On (23h) (Only for Test Purposes)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	APON	0	↑	1	0	0	1	0	0	0	1	1	(23h)
0	Parameter	No Parameter											

Description

This command is only used for test purpose e.g. pixel response time (on/off) measurements on the passive matrix display. Therefore, it is possible that this command is not used for final product software.

All driver outputs become “High” data state and display becomes white.

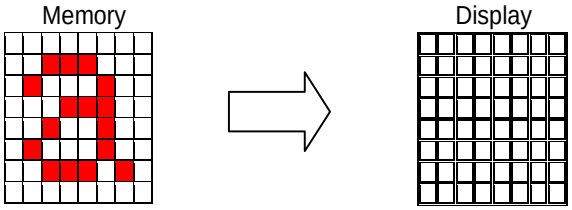
This command makes no change of contents of display memory.

This command does not change any other status.

Exit commands are “All Pixels Off”, “Normal Display Mode On” and “Partial Display On”.

The display is showing the contents of the frame memory after “Normal Display Mode On” and “Partial Display On” commands.

(Example)



Restriction

This command has no effect when module is already All Pixel On mode.

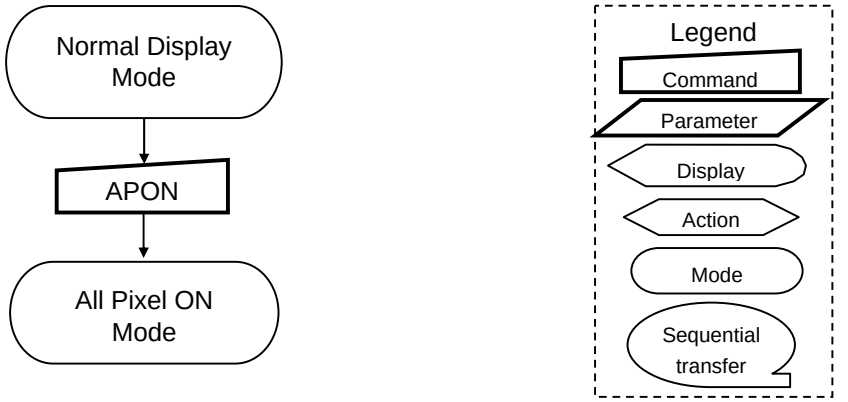
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All pixel on mode disable
S/W Reset	All pixel on mode disable
H/W Reset	All pixel on mode disable

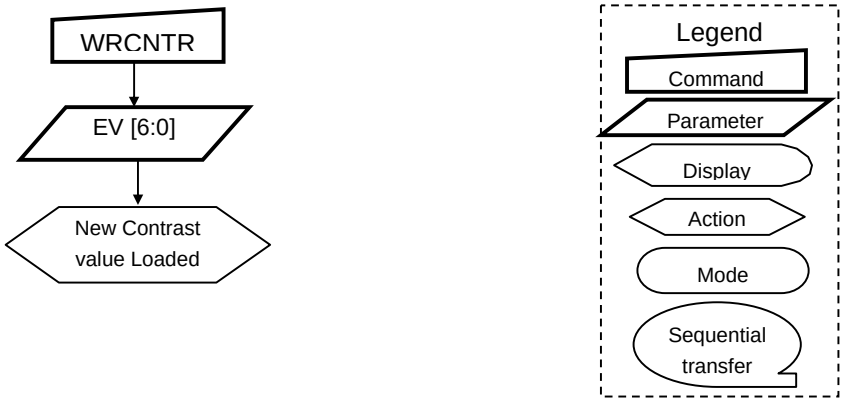
Flow Chart



6.1.16 WRCNTR: Write Contrast (3Fh)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	WRCNTR	0	↑	1	0	0	1	0	0	1	0	1	(25h)
0	Parameter	1	↑	1	-	EV6	EV5	EV4	EV3	EV2	EV1	EV0	-

NOTE: "-" Don't care

Description	This command is used to fine tuning the contrast of the current display. This contrast values can effect segment and common outputs. Parameter range: 0-127dec. MSB is EV6 and LSB is EV0. Default value: 63dec (3Fh)
Restriction	-
Register Availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status: Default Value Power On Sequence: 3Fh S/W Reset: 3Fh H/W Reset: 3Fh
Flow Chart	

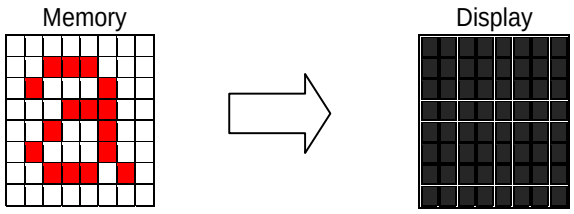
6.1.17 DISPOFF: Display Off (28h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	DISPOFF	0	↑	1	0	0	1	0	1	0	0	0	(28h)
0	Parameter	No Parameter											

Description

This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disables and blank page inserted.
This command makes no change of contents of frame memory.
This command does not change any other status.
There will be no abnormal visible effect on the display.
Exit from this command by Display On (29h)

(Example)



Restriction

This command has no effect when module is already in Display Off mode.

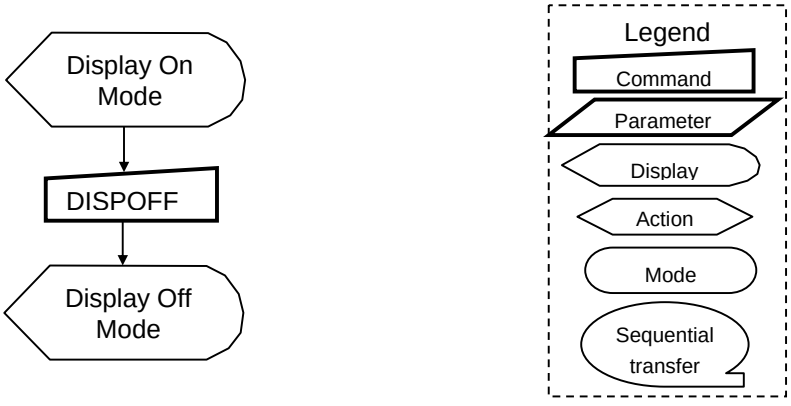
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



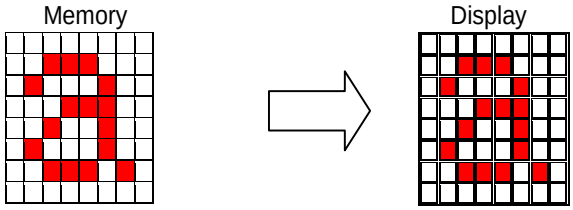
6.1.18 DISPON: Display On (29h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	DISPON	0	↑	1	0	0	1	0	1	0	0	1	(29h)
0	Parameter	No Parameter											

Description

This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.

(Example)



Restriction

This command has no effect when module is already in Display On mode.

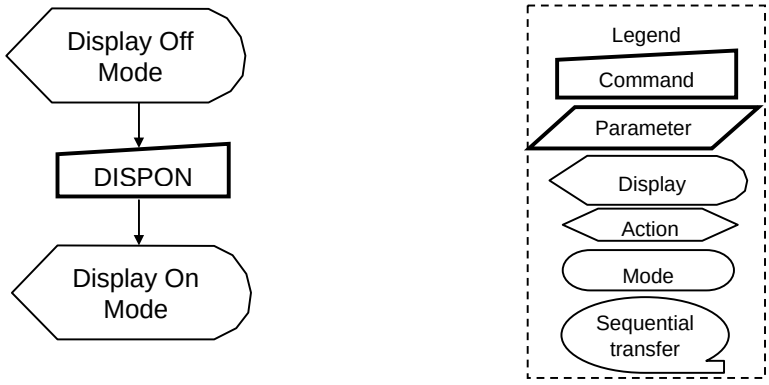
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



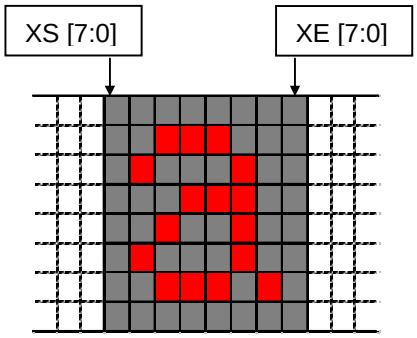
6.1.19 CASET: Column Address Set (2Ah)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	CASET	0	↑	1	0	0	1	0	1	0	1	0	(2Ah)
0	1st Parameter	1	↑	1	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	-
0	2nd Parameter	1	↑	1	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	-

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The value of XS [7:0] and XE [7:0] are referred when RAMWR command comes.
Each value represents one column line in the Frame Memory.

(Example)



Restriction

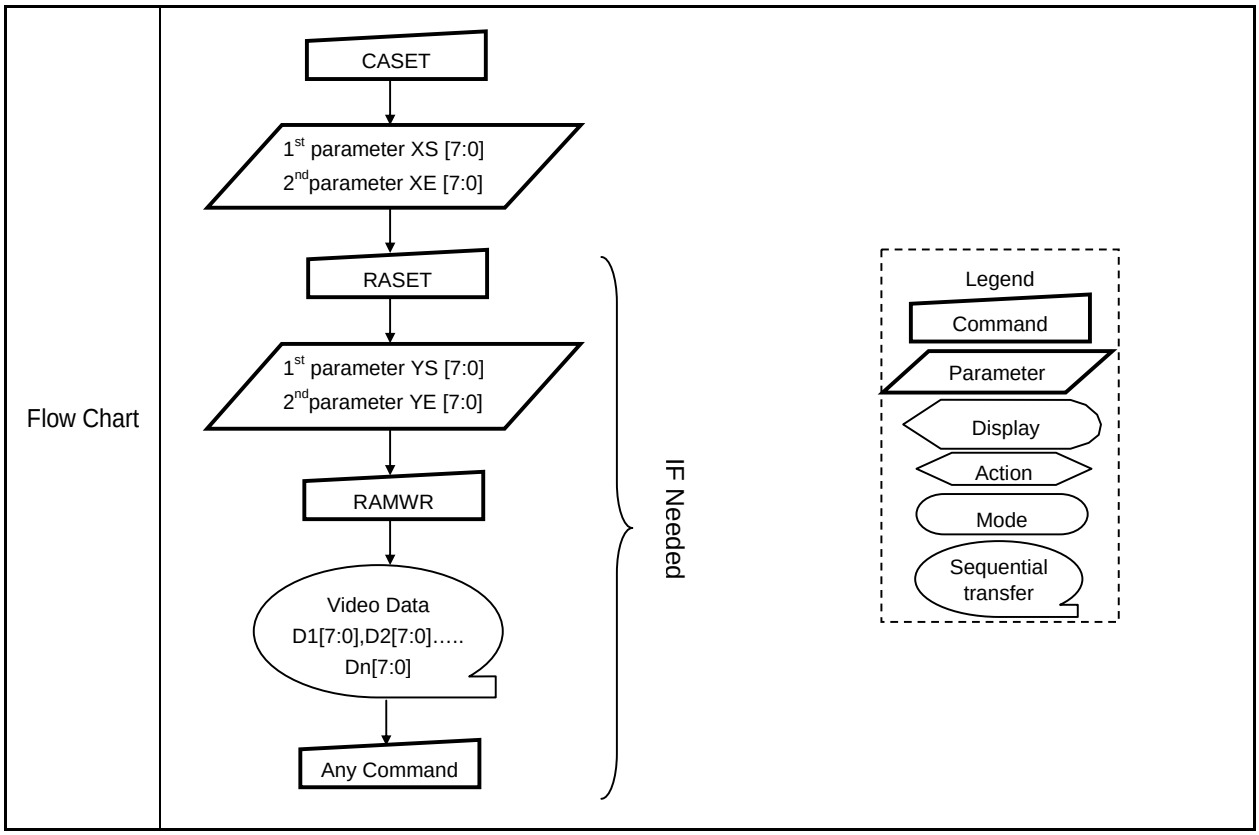
XS [7:0] always must be equal to or less than XE [7:0]
When XS [7:0] or XE [7:0] is greater than 83h, data of out of range will be ignored.
(Parameter range: 0 ≤ XS [7:0] ≤ XE [7:0] ≤ 131(83h))

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	XS [7:0]	XE [7:0]
Power On Sequence	01h (1d)	82h (130d)
S/W Reset	01h (1d)	82h (130d)
H/W Reset	01h (1d)	82h (130d)


Flow Chart
CASET
1st parameter XS [7:0]
2nd parameter XE [7:0]
RASET
1st parameter YS [7:0]
2nd parameter YE [7:0]
RAMWR
Video Data
D1[7:0],D2[7:0].....
Dn[7:0]
Any Command
IF Needed
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

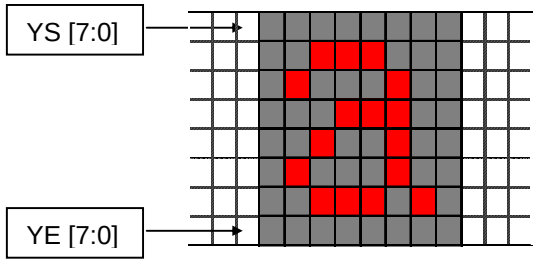
6.1.20 RASET: Row Address Set (2Bh)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	RASET	0	↑	1	0	0	1	0	1	0	1	1	(2Bh)
0	1st parameter	1	↑	1	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	-
0	2nd parameter	1	↑	1	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	-

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The value of YS [7:0] and YE [7:0] are referred when RAMWR command comes.
Each value represents one column line in the Frame Memory.

(Example)



Restriction

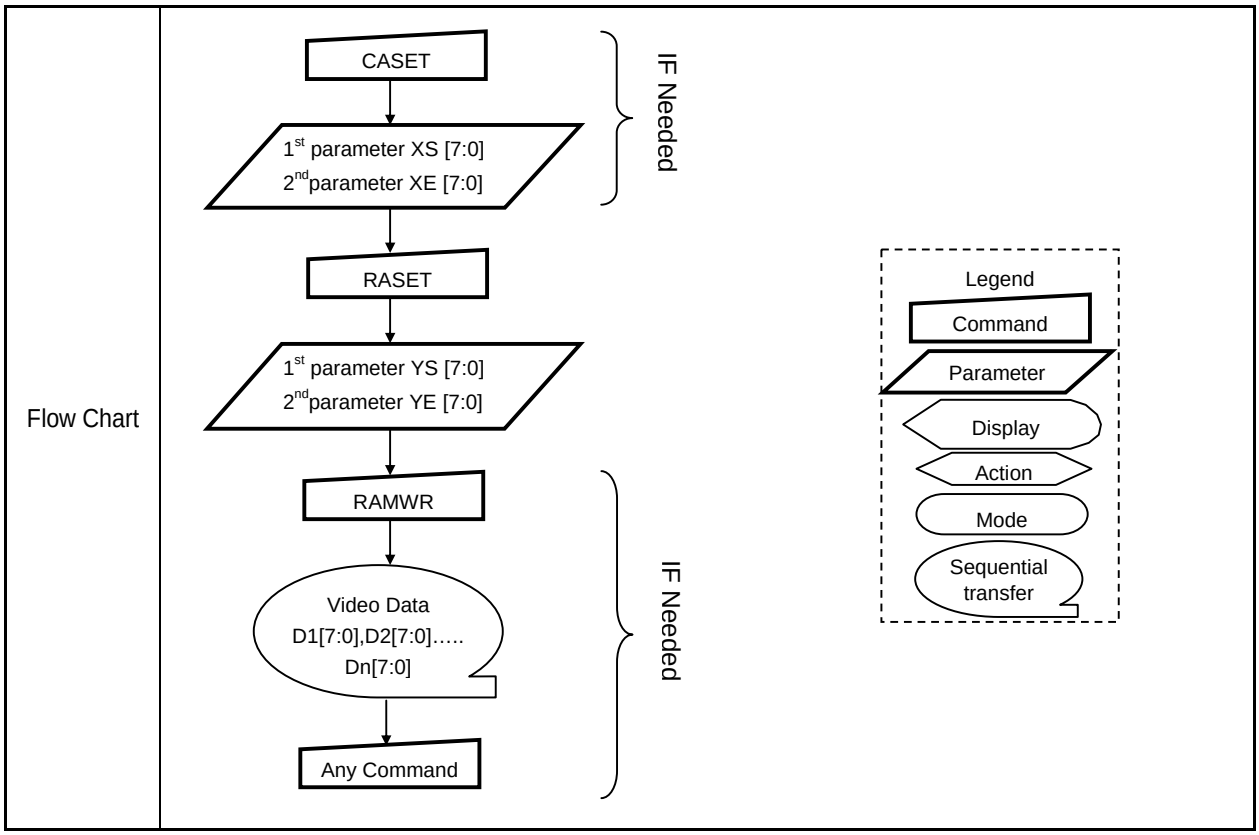
YS [7:0] always must be equal to or less than YE [7:0]
When YS [7:0] or YE [7:0] is greater than 83h, data of out of range will be ignored.
(Parameter range: 0 ≤ YS [7:0] ≤ YE [7:0] ≤ 131(83h))

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	YS [7:0]	YE [7:0]
Power On Sequence	01h (1d)	82h (130d)
S/W Reset	01h (1d)	82h (130d)
H/W Reset	01h (1d)	82h (130d)


Flow Chart
CASET
1st parameter XS [7:0]
2nd parameter XE [7:0]
IF Needed
RASET
1st parameter YS [7:0]
2nd parameter YE [7:0]
RAMWR
Video Data
D1[7:0],D2[7:0].....
Dn[7:0]
Any Command
IF Needed
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.1.21 RAMWR: Memory Write (2Ch)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	RAMWR	0	↑	1	0	0	1	0	1	1	0	0	(2Ch)
0	Data write	1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	-
:	:	:	:	:	:	:	:	:	:	:	:	:	:
0	Data write	1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	-

Description

This command is used to transfer data MCU to frame memory.
This command makes no change to the other driver status.
When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.
The Start Column/Start Row positions are different in accordance with MADCTL setting. (See section 5.2.2)
Then D[7:0] is stored in frame memory and the column register and the row register incremented as in Fig. 5.2.1.
Frame Write can be canceled by sending any other command.

Restriction

In all color modes, there is no restriction on length of parameters.

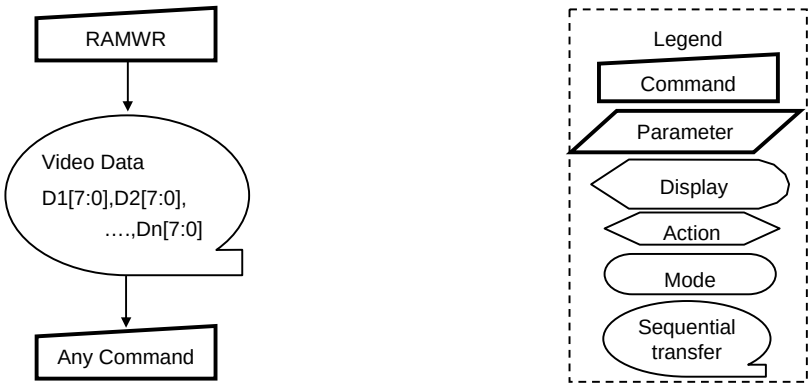
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is remained
H/W Reset	Contents of memory is remained

Flow Chart



6.1.22 RAMRD: Memory Read (2Eh)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	RAMRD	0	↑	1	0	0	1	0	1	1	1	0	(2Eh)
0	Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
0	Data read	1	1	↑	D7	D6	D5	D4	D3	D2	D1	D0	-
:	:	:	:	:	:	:	:	:	:	:	:	:	:
0	Data read	1	1	↑	D7	D6	D5	D4	D3	D2	D1	D0	-

Description

This command is used to transfer data from frame memory to MCU.
This command makes no change to the other driver status.
When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.
The Start Column/Start Row positions are different in accordance with MADCTL setting. (See section 5.2.2)
Then D[7:0] is read back from the frame memory and the column register and the row register incremented as in Fig. 5.2.1.
Frame Read can be canceled by sending any other command.

Restriction

In all color modes, the Frame Read is always 12-bit so there is no restriction on length of parameters.
Note-Memory Read is only possible via the Parallel Interface.

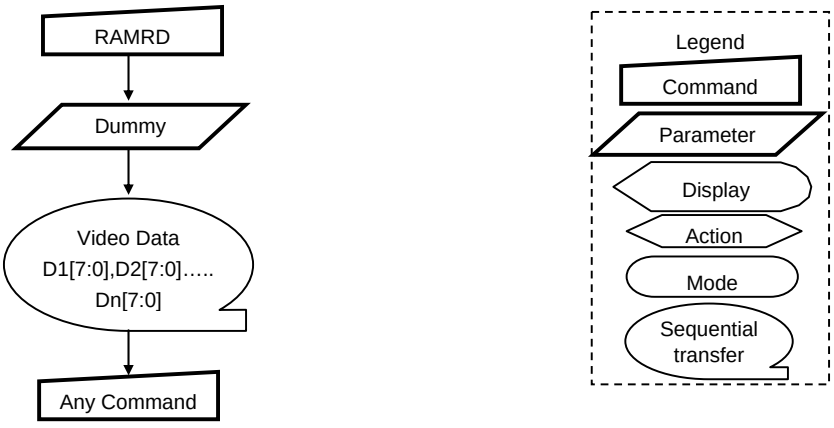
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is remained
H/W Reset	Contents of memory is remained

Flow Chart



6.1.23 RGBSET: Colour Set for 256-Color Display (2Dh)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	RGBSET	0	↑	1	0	0	1	0	1	1	0	1	(2Dh)
0	1st parameter	1	↑	1	-	-	-	-	R03	R02	R01	R00	-
0	:	1	↑	1	-	-	-	-	Rn3	Rn2	Rn1	Rn0	-
0	8th parameter	1	↑	1	-	-	-	-	R73	R72	R71	R70	-
0	9th parameter	1	↑	1	-	-	-	-	G03	G02	G01	G00	-
0	:	1	↑	1	-	-	-	-	Gn3	Gn2	Gn1	Gn0	-
0	16th parameter	1	↑	1	-	-	-	-	G73	G72	G71	G70	-
0	17th parameter	1	↑	1	-	-	-	-	B03	B02	B01	B00	-
0	:	1	↑	1	-	-	-	-	Bn3	Bn2	Bn1	Bn0	-
0	20th parameter	1	↑	1	-	-	-	-	B33	B32	B31	B30	-

Description

This command is used to define the LUT for 8bit-to-12bit color depth conversations. (See also section 5.2.7)
20 Bytes must be written to the LUT regardless of the color mode. Only the values in Section 5.2.7 are referred.
This command has no effect on other commands/parameters and Contents of frame memory.
Visible change takes effect next time the Frame Memory is written to.

Restriction

Do not send any command before the last data is sent or LUT is not defined correctly.

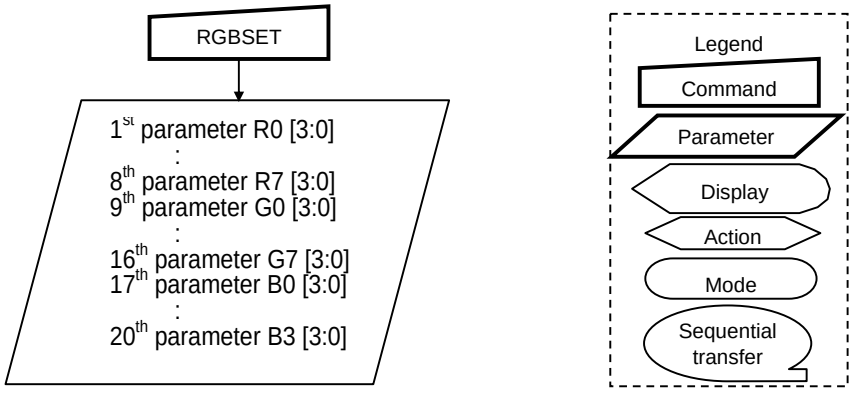
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Random values
S/W Reset	Contents of the look-up table protected
H/W Reset	Random values

Flow Chart



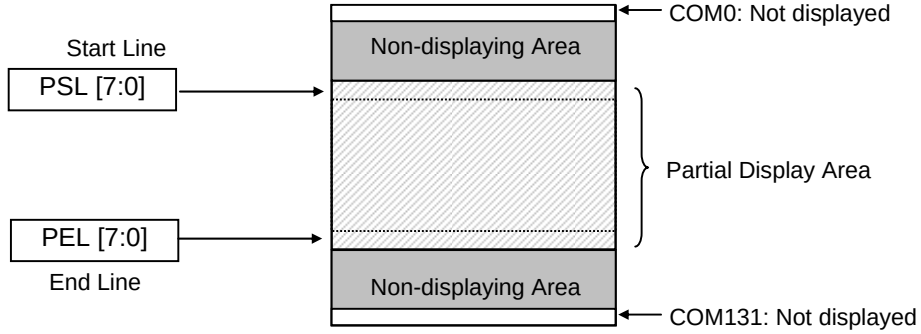
6.1.24 PTLAR: Partial Area (30h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	PTLAR	0	↑	1	0	0	1	1	0	0	0	0	(30h)
0	1st parameter	1	↑	1	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-
0	2nd parameter	1	↑	1	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	-

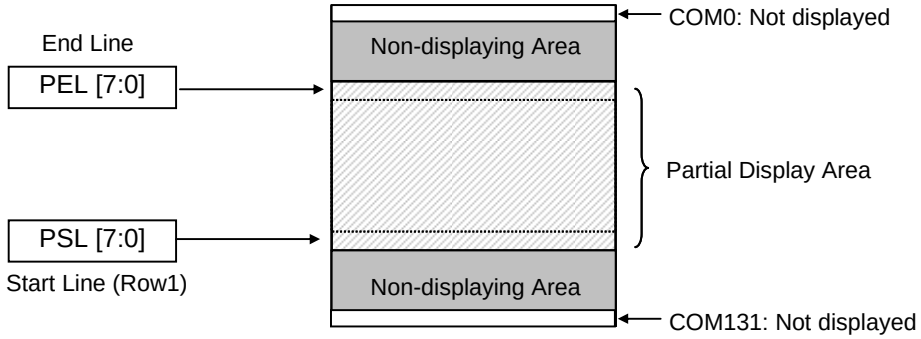
Description

This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Line (PSL) and the second the End Line (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory Line counter.

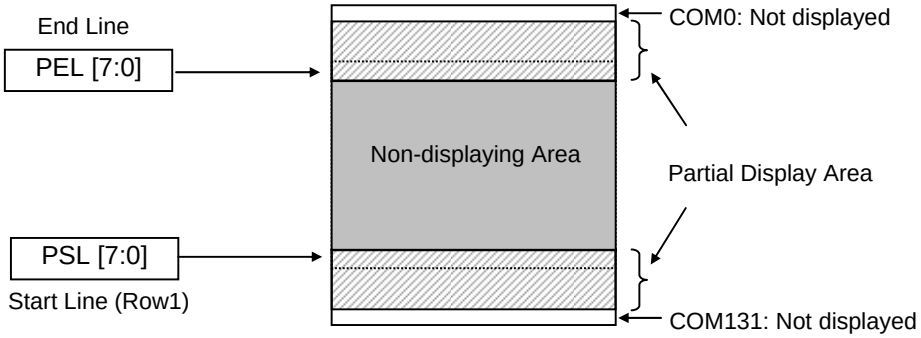
If End Line > Start Line when MADCTL ML=0:



If End Line > Start Line when MADCTL ML=1:



If End Line < Start Line when MADCTL ML=0:



* Row1: Frame memory row address 1.

If End Line = Start Line then the Partial Area will be one block (4-line) deep.

Restriction

PSL[7:0] and PEL[7:0] is based on block(4-line) unit, so, lower 2-bits (PSL[1:0], PEL[1:0]) are always assumed to 0.

PSL[7:0]=00h, 04h, 08h, 0Ah, … , 80h

PEL[7:0]= 00h, 04h, 08h, 0Ah, … , 80h

PSL[7:0] and PEL[7:0] have offset address (-4) in this driver.

So, to display COM0 to COM32 in partial mode partial address should be PSL[7:0] = 80h, PEL[7:0] = 28h

Register Availability

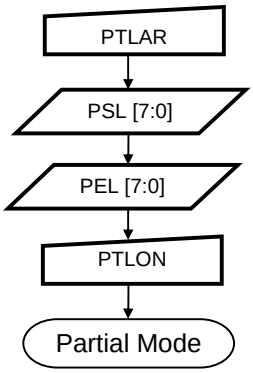
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

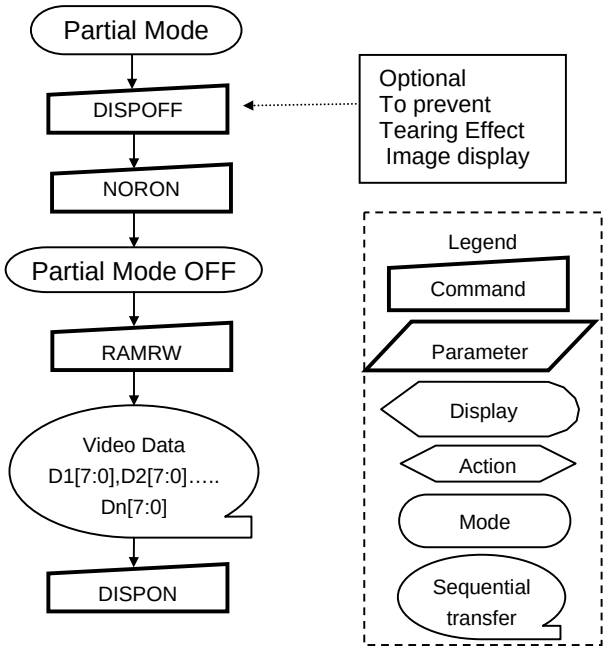
Status	Default Value	
	PSL [7:0]	PEL [7:0]
Power On Sequence	00h	80h
S/W Reset	00h	80h
H/W Reset	00h	80h

Flow Chart

1. To Enter Partial Mode



2. To Exit Partial Mode



6.1.25 SCRLAR: Scroll Area (33h) (Not used: Removed in this driver)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	SCRLAR	0	↑	1	0	0	1	1	0	0	1	1	(33h)
0	1st parameter	1	↑	1	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-
0	2nd parameter	1	↑	1	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	-
0	3rd parameter	1	↑	1	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	-

Description

This command defines the Vertical Scrolling Area of the display.

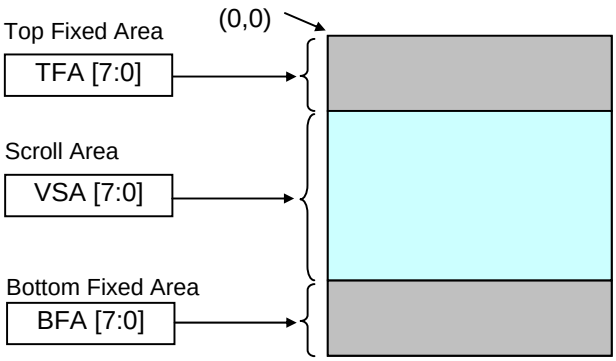
When MADCTL ML=0

The 1st parameter TFA [7:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 2nd parameter VSA [7:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) The first line appears immediately after the bottom most line of the Top Fixed Area.

The 3rd parameter BFA [7:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



Restriction

The condition is (TFA+VSA+BFA) ≥130, otherwise Scrolling mode is undefined.

In Vertical Scroll Mode, MADCTL parameter MV should be set to '0'-this only affects the Frame Memory Write.

TFA[7:0], VSA[7:0] and BFA[7:0] is based on 1-line unit.

TFA[7:0]= 00h, 01h, 02h, 03h, … , 84h

VSA[7:0]= 00h, 01h, 02h, 03h, … , 84h

BFA[7:0]= 00h, 01h, 02h, 03h, … , 84h

Register Availability

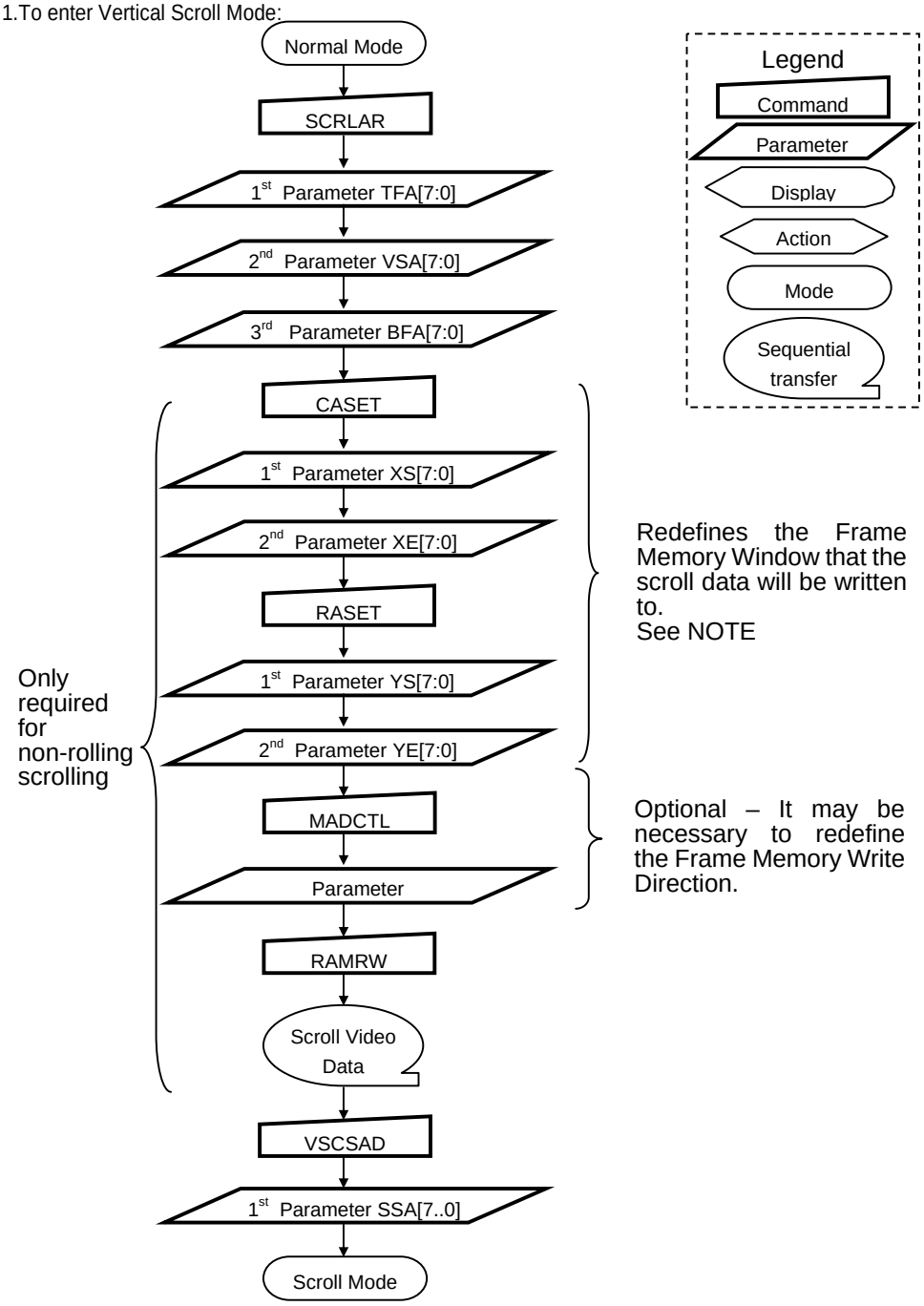
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	TFA [7:0]	VSA [7:0]	BFA [7:0]
Power On Sequence	00h	84h	00h
S/W Reset	00h	84h	00h
H/W Reset	00h	84h	00h

Flow Chart

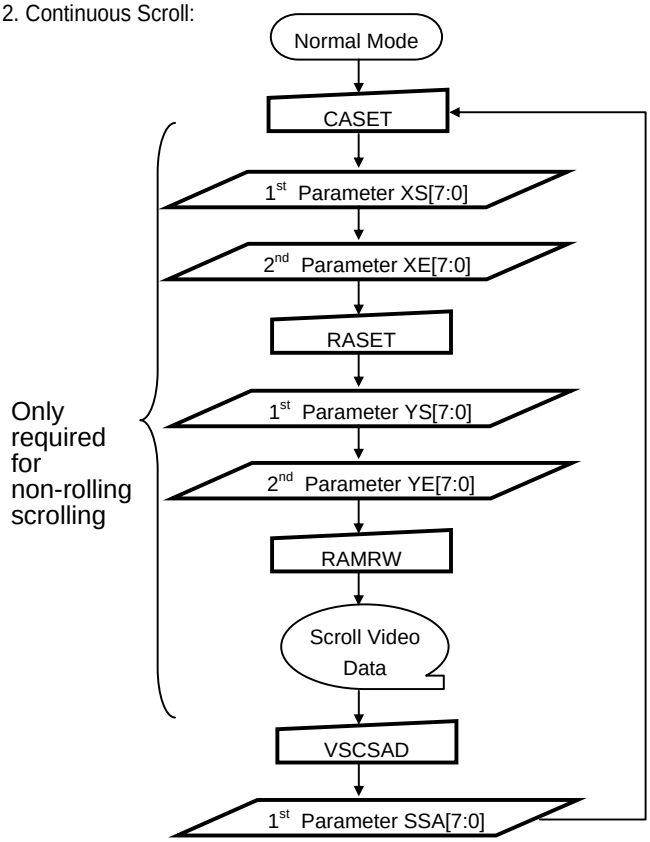
1.To enter Vertical Scroll Mode:

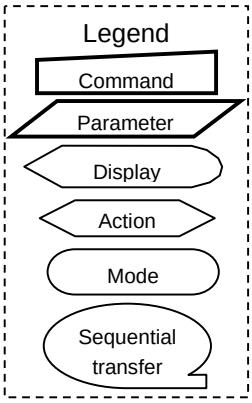


NOTE: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

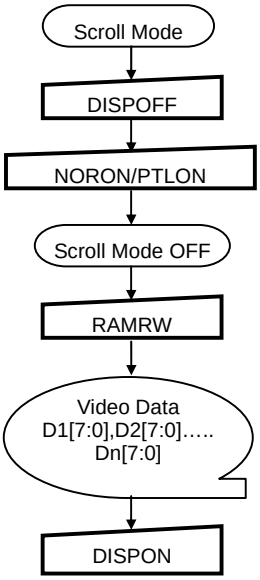
Flow Chart

2. Continuous Scroll:





3. To Exit Vertical Scroll Mode:



NOTE: Scroll Mode can be exit by both the Normal Display Mode On(13h) and Partial Mode On (12h) commands.

6.1.26 TEOFF: Tearing Effect Line OFF (34h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	TEOFF	0	↑	1	0	0	1	1	0	1	0	0	(34h)
0	Parameter	No Parameter											

Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
Restriction	This command has no effect when Tearing Effect output is already OFF.

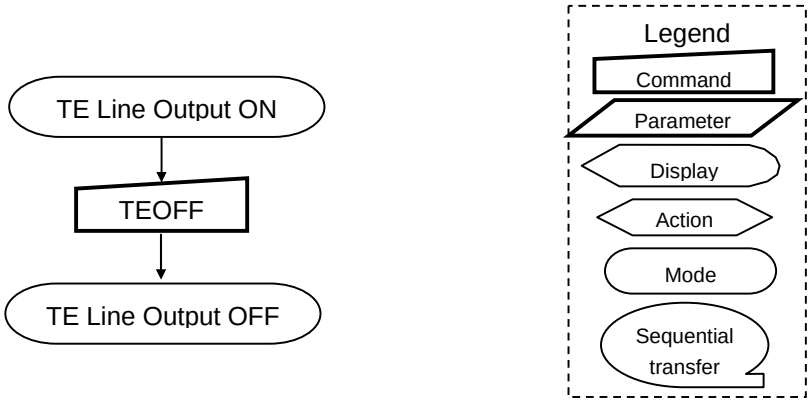
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing effect off
S/W Reset	Tearing effect off
H/W Reset	Tearing effect off

Flow Chart



6.1.27 TEON: Tearing Effect Line ON (35h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	TEON	0	↑	1	0	0	1	1	0	1	0	1	(35h)
0	Parameter	1	↑	1	-	-	-	-	-	-	-	M	-

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit ML.
The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-"=Don't Care).
See section 5.2.6 for more information.
Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already OFF.

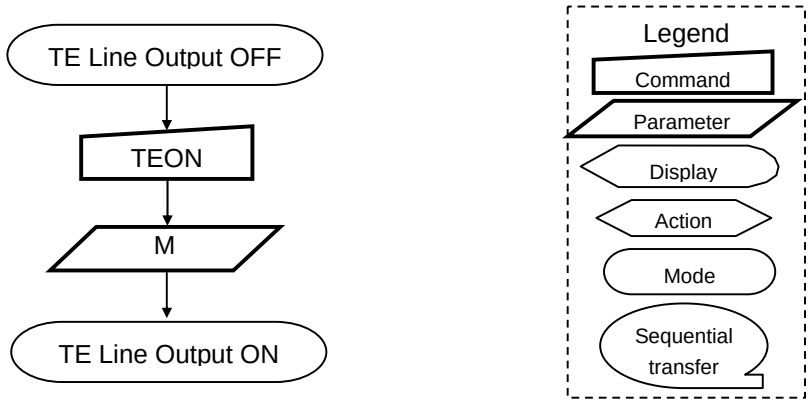
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing effect off & M=0
S/W Reset	Tearing effect off & M=0
H/W Reset	Tearing effect off & M=0

Flow Chart



6.1.28 MADCTR: Memory Data Access Control (36h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	MADCTR	0	↑	1	0	0	1	1	0	1	1	0	(36h)
0	Parameter	1	↑	1	MY	MX	MV	ML	RGB	-	-	-	-

Description

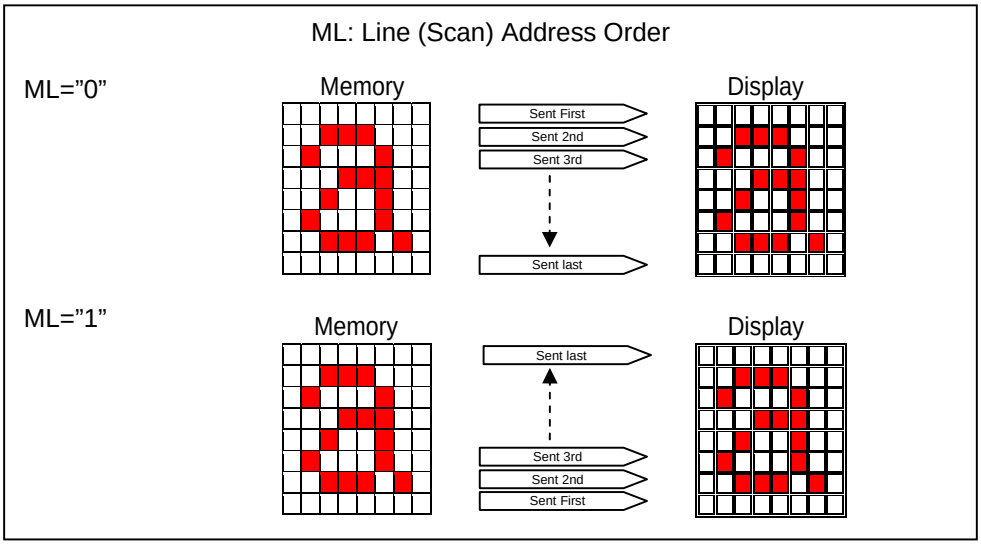
This command defines read/write scanning direction of frame memory.

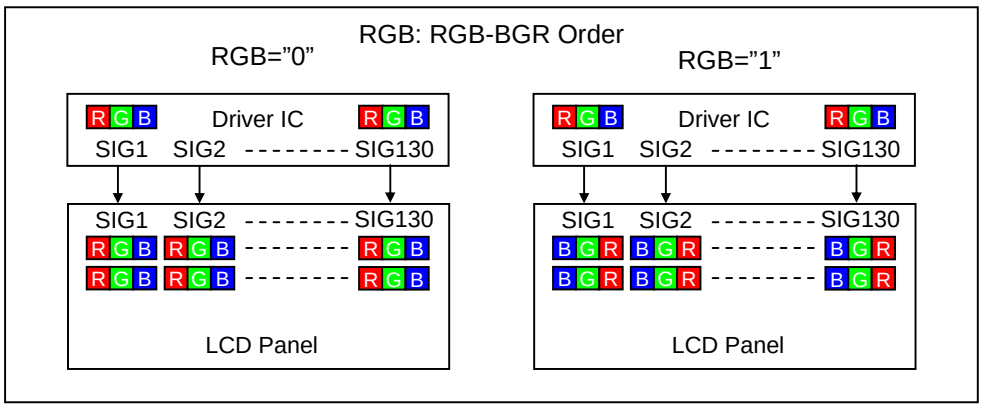
This command makes no change on the other driver status.

Note: B4 affects to Partial Area (30h), Vertical Scrolling Definition (33h), Vertical Scrolling Start address (37h), Partial On (12h) commands

Bit Assignment

Bit	NAME	DESCRIPTION
MY	ROW ADDRESS ORDER	These 3bits controls MCU to memory write/read direction. (See Section 5.2.2 “MCU to memory write/read direction”)
MX	COLUMN ADDRESS ORDER	
MV	ROW/COLUMN SELECTION	
ML	LINE ADDRESS ORDER	LCD refresh direction control
RGB	RGB-BGR ORDER	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)





Restriction

D2, D1 and D0 of the 1st parameter are set to ‘000’internally.

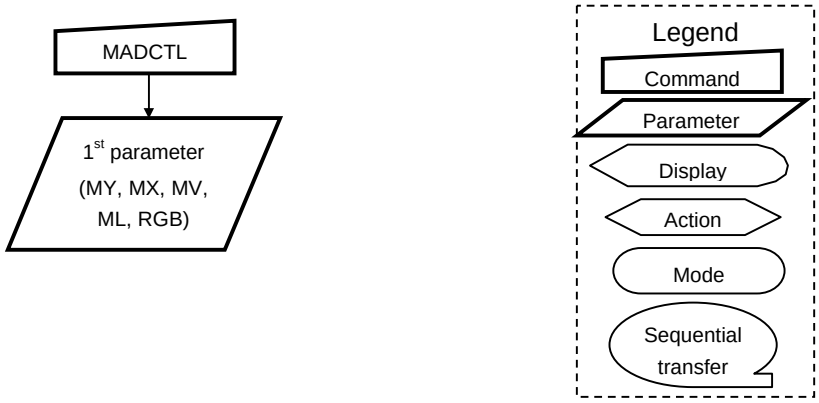
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0
S/W Reset	No Change
H/W Reset	MY=0,MX=0,MV=0,ML=0,RGB=0

Flow Chart



6.1.29 VSCSAD: Vertical Scroll Start Address of RAM (37h) (Not used: Removed in this driver)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	VSCSAD	0	↑	1	0	0	1	1	0	1	1	1	(37h)
0	Parameter	1	↑	1	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	-

Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.

The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

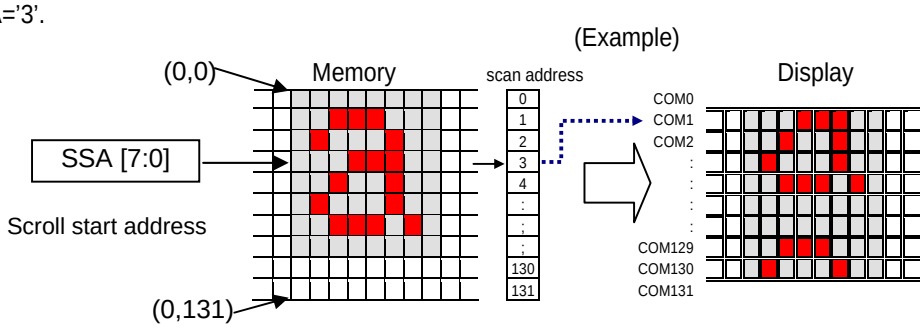
This command Start the scrolling.

Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h).

When MADCTL ML=0

Example:

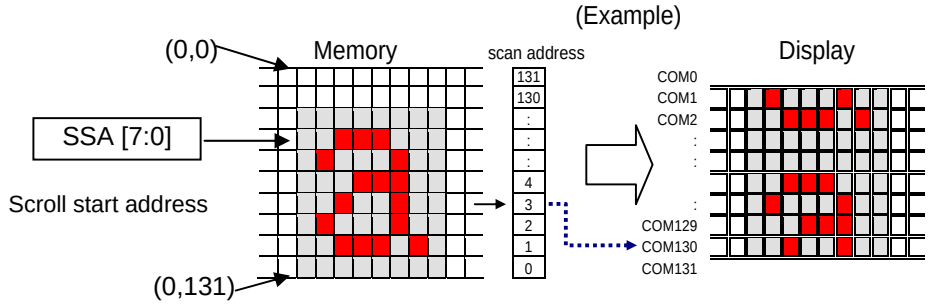
When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=130 and Vertical Scrolling Pointer SSA='3'.



When MADCTL ML =1

Example:

When Top Fixed Area= Bottom Fixed Area=00, Vertical Scrolling Area=130 and SSA='3'



NOTE: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

SSA refers to the Frame Memory line Pointer.

Restriction

Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)-otherwise undesirable image will be displayed on the Panel.

SSA[7:0] is based on 1-line unit.

SSA[7:0] = 00h, 01h, 02h, 03h, … , 83h

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00</td></tr>
<tr><td>S/W Reset</td><td>00</td></tr>
<tr><td>H/W Reset</td><td>00</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

6.1.30 IDMOFF: Idle Mode Off (38h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	IDMOFF	0	↑	1	0	0	1	1	1	0	0	0	(38h)
0	Parameter	No Parameter											

Description

This command is used to recover from Idle mode on.
There will be no abnormal visible effect on the display mode change transition.
In the idle off mode,

1. LCD can display maximum 4k colors.
2. Normal frame frequency is applied.

Restriction

This command has no effect when module is already in idle off mode.

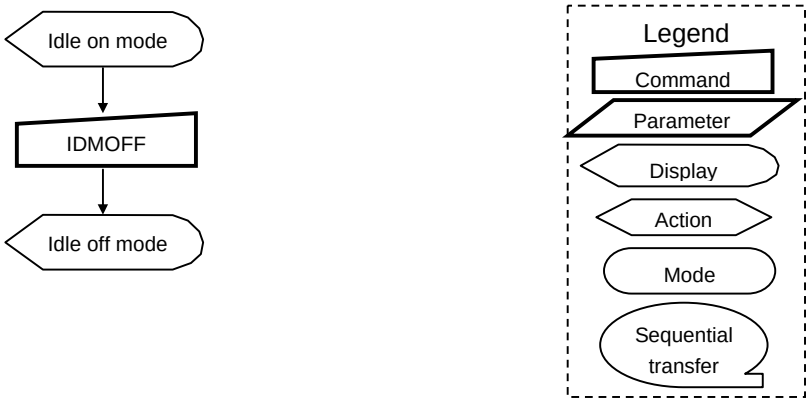
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode off
S/W Reset	Idle mode off
H/W Reset	Idle mode off

Flow Chart



6.1.31 IDMON: Idle Mode On (39h)

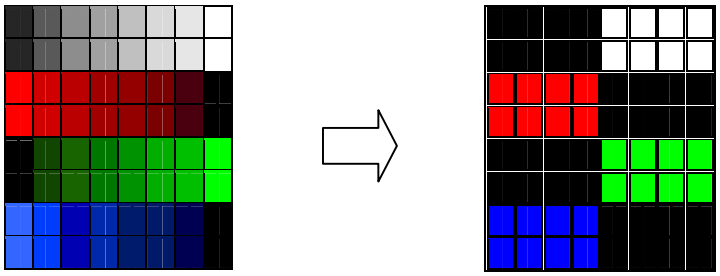
ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	IDMON	0	↑	1	0	0	1	1	1	0	0	1	(39h)
0	Parameter	No Parameter											

Description

This command is used to enter into Idle mode on.
There will be no abnormal visible effect on the display mode change transition.
In the idle on mode,
1. Color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command

(Example)

Memory → Display



"X": don't care

Color	$R_3\ R_2\ R_1\ R_0$	$G_3\ G_2\ G_1\ G_0$	$B_3\ B_4\ B_1\ B_0$
Black	0XXX	0XXX	0XXX
Blue	0XXX	0XXX	1XXX
Red	1XXX	0XXX	0XXX
Magenta	1XXX	0XXX	1XXX
Green	0XXX	1XXX	0XXX
Cyan	0XXX	1XXX	1XXX
Yellow	1XXX	1XXX	0XXX
White	1XXX	1XXX	1XXX

Restriction

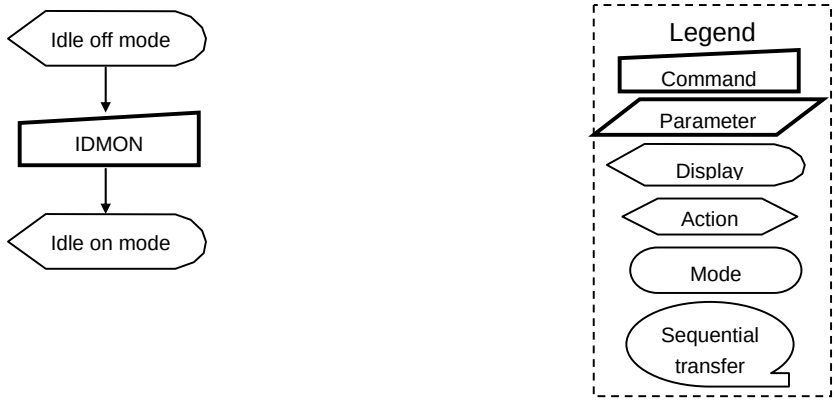
This command has no effect when module is already in idle on mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode off
S/W Reset	Idle mode off
H/W Reset	Idle mode off

Flow Chart	

Idle off mode
IDMON
Idle on mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.1.32 COLMOD: Interface Pixel Format (3Ah)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	COLMOD	0	↑	1	0	0	1	1	1	0	1	0	(3Ah)
0	Parameter	1	↑	1	-	-	-	-	-	P2	P1	P0	-

Description

This command is used to define the format of RGB picture data, which is to be transferred via the MCU Interface. The formats are shown in the table.

Interface Format	D2	D1	D0
Not Defined	0	0	0
Not Defined	0	0	1
8Bit/Pixel	0	1	0
12Bit/Pixel (Type A)	0	1	1
Not Defined	1	0	0
16Bit/Pixel	1	0	1
12Bit/Pixel (Type B)	1	1	0
Not Defined	1	1	1

NOTE: In 8 Bit/Pixel mode, the LUT is applied to transfer data into the Frame Memory.

The 16bit/pixel format is dithered to 12bit/pixel to transfer data into Frame Memory

Restriction

There is no visible effect until the Frame Memory is written to.

Register Availability

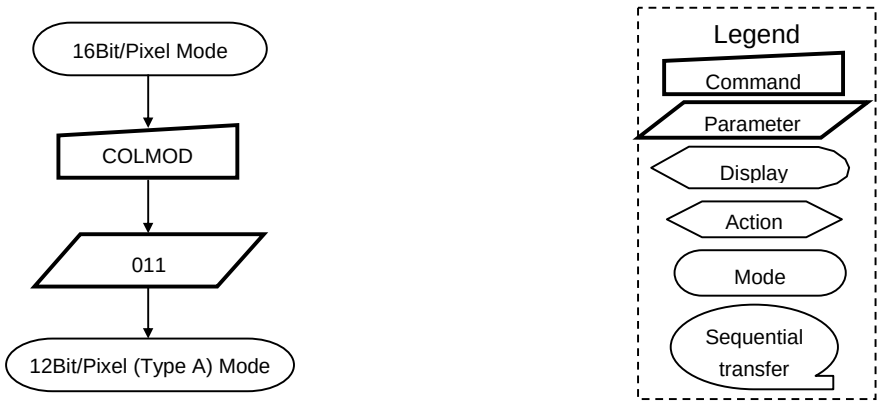
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	12Bit/Pixel (Type A)
S/W Reset	No Change
H/W Reset	12Bit/Pixel (Type A)

Flow Chart

Example:



6.1.33 RDID1: Read ID1 Value (DAh)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	RDID1	0	↑	1	1	1	0	1	1	0	1	0	(DAh)
0	Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
0	2nd Parameter	1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-

Description

This read byte returns 8-bit LCD module's manufacturer ID

The 1st parameter is dummy data

The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.

NOTE: See command RDDID (04h), 2nd parameter.

Restriction

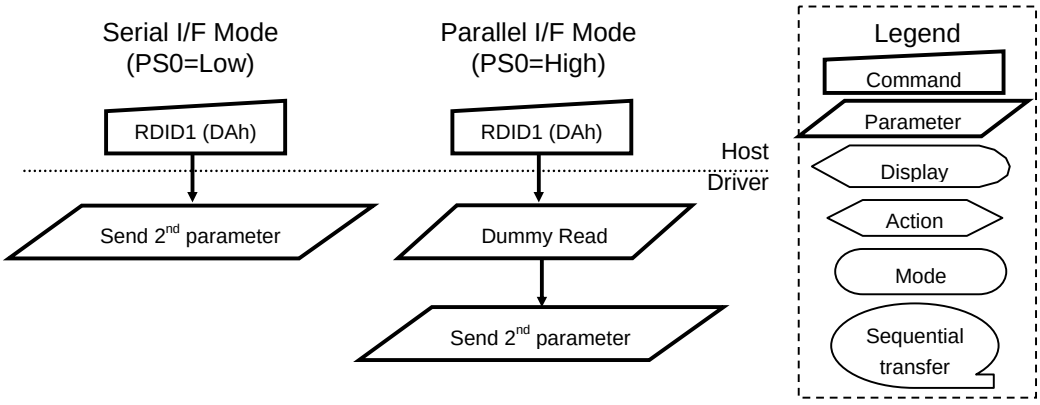
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	45h
S/W Reset	45h
H/W Reset	45h

Flow Chart



6.1.34 RDID2: Read ID2 Value (DBh)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	RDID2	0	↑	1	1	1	0	1	1	0	1	1	(DBh)
0	Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
0	2nd Parameter	1	1	↑	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-

Description

This read byte returns 8-bit LCD module/driver version ID
The 1st parameter is dummy data
The 2nd parameter (ID26 to ID20): LCD module/driver version ID
Parameter Range: ID=80h to FFh
NOTE: See command RDDID (04h), 3rd parameter.

Restriction

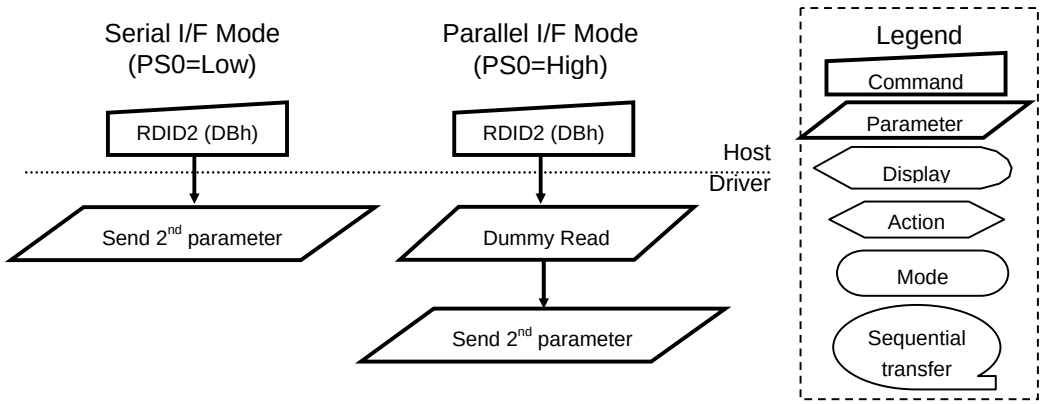
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	80 ~ FFh (Not Fixed)
S/W Reset	80 ~ FFh (Not Fixed)
H/W Reset	80 ~ FFh (Not Fixed)

Flow Chart



6.1.35 RDID3: Read ID3 Value (DCh)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	RDID3	0	↑	1	1	1	0	1	1	1	0	0	(DCh)
0	Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
0	2nd Parameter	1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

Description

This read byte returns 8-bit LCD module/driver ID.
The 1st parameter is dummy data
The 2nd parameter (ID37 to ID30): LCD module/driver ID.
NOTE: See command RDDID (04h), 4th parameter.

Restriction

-

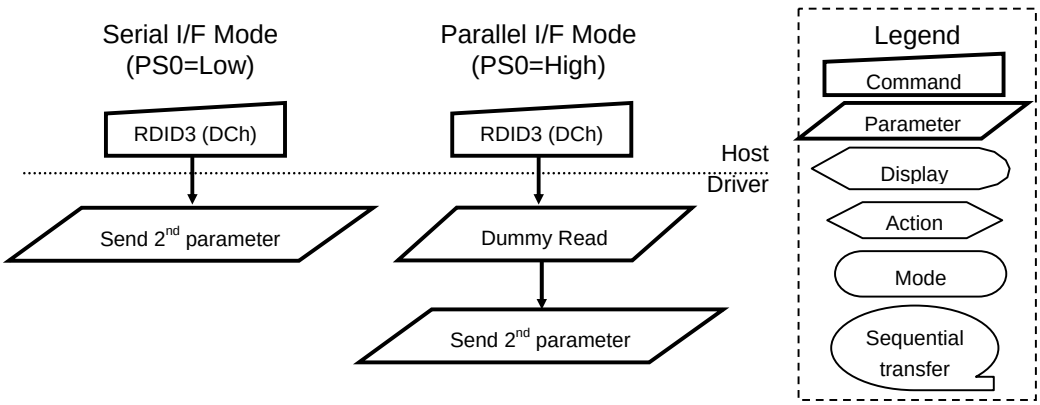
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	03h
S/W Reset	03h
H/W Reset	03h

Flow Chart



6.1.36 CLKINT: Internal Oscillator (B0h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	CLKINT	0	↑	1	1	0	1	1	0	0	0	0	(B0h)
0	Parameter	No Parameter											

Description	Select and using internal oscillator.
Restriction	-

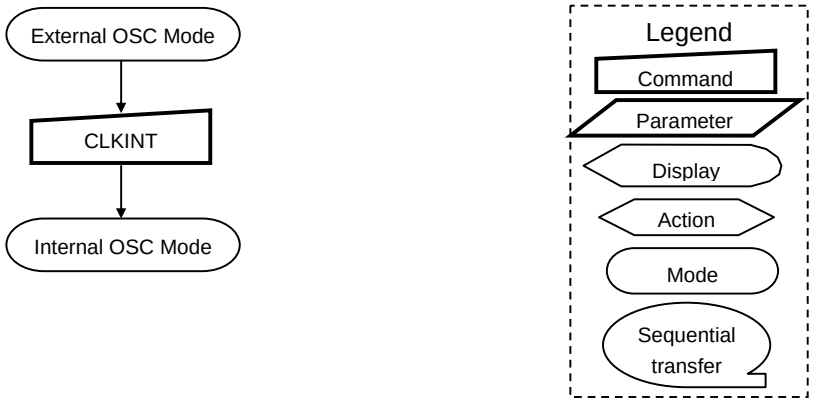
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Internal OSC mode
S/W Reset	Internal OSC mode
H/W Reset	Internal OSC mode

Flow Chart



6.1.37 CLKEXT: External Oscillator (B1h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	CLKEXT	0	↑	1	1	0	1	1	0	0	0	1	(B1h)
0	Parameter	No Parameter											

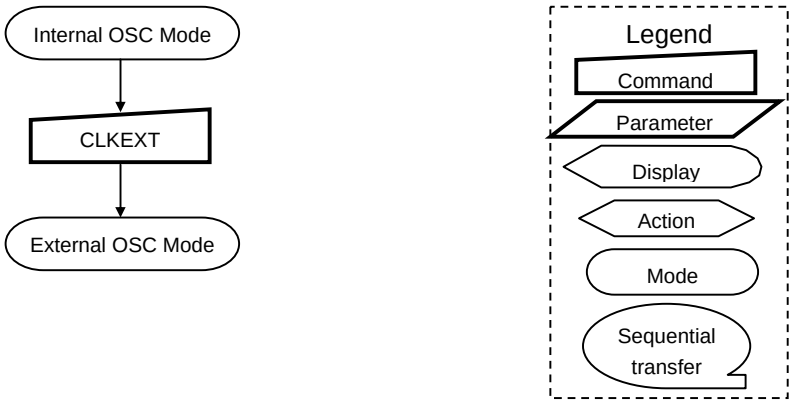
Description	Select and using external oscillator. When an external oscillator is used the external oscillator is connected to the OSC pad.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Internal OSC mode
S/W Reset	Internal OSC mode
H/W Reset	Internal OSC mode

Flow Chart



6.1.38 FRMSEL: Frame frequency in normal mode (B4h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	FRMSEL	0	↑	1	1	0	1	1	0	1	0	0	(B4h)
0	1st parameter	1	↑	1	-	-	-	FA4	FA3	FA2	FA1	FA0	-
0	2nd parameter	1	↑	1	-	-	-	FB4	FB3	FB2	FB1	FB0	-
0	3rd parameter	1	↑	1	-	-	-	FC4	FC3	FC2	FC1	FC0	-
0	4th parameter	1	↑	1	-	-	-	FD4	FD3	FD2	FD1	FD0	-

Description

Select frame frequency in normal display mode.

1st parameter: Frame frequency value set in TEMP range 0(–35°C) to TA
2nd parameter: Frame frequency value set in TEMP range TA to TB
3rd parameter: Frame frequency value set in TEMP range TB to TC
4th parameter: Frame frequency value set in TEMP range TC to 127(92°C)

*NOTE: For the relationship between FA[4:0] ~ FD[4:0] and frame frequency, see "**Table 6.1.4**"*

*For more detail about frequency adjustment method, see section "*5.11.9.3 Frame Frequency Adjustment*".*

Restriction

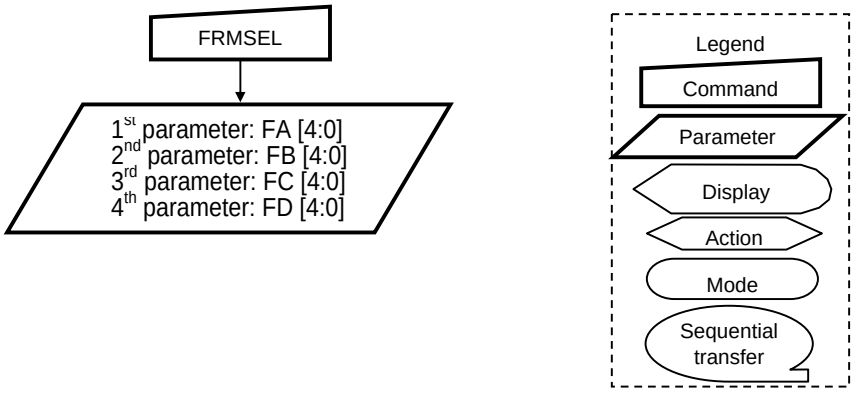
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	FA [4:0]	FB [4:0]	FC [4:0]	FD [4:0]
Power On Sequence	03h (46Hz)	07h (66Hz)	07h (66Hz)	07h (66Hz)
S/W Reset	03h (46Hz)	07h (66Hz)	07h (66Hz)	07h (66Hz)
H/W Reset	03h (46Hz)	07h (66Hz)	07h (66Hz)	07h (66Hz)

Flow Chart



6.1.39 FRM8SEL: Frame frequency in idle mode (8-color mode) (B5h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	FRM8SEL	0	↑	1	1	0	1	1	0	1	0	1	(B5h)
0	1st parameter	1	↑	1	-	-	-	F8A4	F8A3	F8A2	F8A1	F8A0	-
0	2nd parameter	1	↑	1	-	-	-	F8B4	F8B3	F8B2	F8B1	F8B0	-
0	3rd parameter	1	↑	1	-	-	-	F8C4	F8C3	F8C2	F8C1	F8C0	-
0	4th parameter	1	↑	1	-	-	-	F8D4	F8D3	F8D2	F8D1	F8D0	-

Description

Select frame frequency in idle display mode (8-color mode).

1st parameter: Frame frequency value set in TEMP range 0(–35°C) to TA
2nd parameter: Frame frequency value set in TEMP range TA to TB
3rd parameter: Frame frequency value set in TEMP range TB to TC
4th parameter: Frame frequency value set in TEMP range TC to 127(92°C)

*NOTE: For the relationship between F8A[4:0] ~ F8D[4:0] and frame frequency, see "**Table 6.1.4**"*

For more detail about frequency adjustment method, see section "5.11.9.3 Frame Frequency Adjustment".

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	F8A[4:0]	F8B[4:0]	F8C[4:0]	F8D[4:0]
Power On Sequence	03h (46Hz)	07h (66Hz)	07h (66Hz)	07h (66Hz)
S/W Reset	03h (46Hz)	07h (66Hz)	07h (66Hz)	07h (66Hz)
H/W Reset	03h (46Hz)	07h (66Hz)	07h (66Hz)	07h (66Hz)

Flow Chart

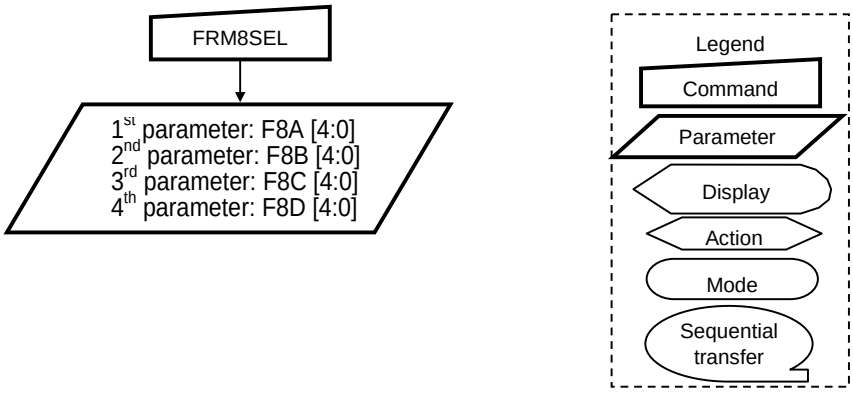


Table 6.1.4 Frame frequency value according to the parameter of FRMSEL (FRM8SEL) command

FA[4:0] to FD[4:0] F8A[4:0] to F8D[4:0]	fFR (frame frequency)	FA[4:0] to FD[4:0] F8A[4:0] to F8D[4:0]	fFR (frame frequency)
0 (00h)	30.1 Hz	16 (10h)	109.8 Hz
1 (01h)	35.2 Hz	17 (11h)	115.4 Hz
2 (02h)	40.0 Hz	18 (12h)	120.3 Hz
3 (03h)	46.1 Hz	19 (13h)	125.5 Hz
4 (04h)	50.0 Hz	20 (14h)	131.3 Hz
5 (05h)	54.9 Hz	21 (15h)	134.8 Hz
6 (06h)	60.1 Hz	22 (16h)	140.9 Hz
7 (07h)	65.7 Hz	23 (17h)	143.8 Hz
8 (08h)	70.4 Hz	24 (18h)	151.4 Hz
9 (09h)	75.7 Hz	25 (19h)	155.9 Hz
10 (0Ah)	79.9 Hz	26 (1Ah)	159.8 Hz
11 (0Bh)	83.9 Hz	27 (1Bh)	164.9 Hz
12 (0Ch)	88.9 Hz	28 (1Ch)	167.8 Hz
13 (0Dh)	95.1 Hz	29 (1Dh)	173.5 Hz
14 (0Eh)	100.0 Hz	30 (1Eh)	177.8 Hz
15 (0Fh)	105.6 Hz	31 (1Fh)	184.5 Hz

During duty selected partial mode, frame frequency will be changed according to the predetermined dividing ratio. (Refer Section 5.11.10)

6.1.40 TMPRNG: Temperature Range Set for Frame Frequency Adjustment (B6h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	TMPRNG	0	↑	1	1	0	1	1	0	1	1	0	(B6h)
0	1st parameter	1	↑	1	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	-
0	2nd parameter	1	↑	1	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	-
0	3rd parameter	1	↑	1	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	-

Description

Temperature range set for automatic frame frequency adjustment operation according the current temperature value.

1st parameter: Temperature range A value set
2nd parameter: Temperature range B value set
3rd parameter: Temperature range C value set

NOTE: For the relationship between TA[6:0] to TC[6:0] and frame frequency, see section "5.11.9.3 Frame Frequency Adjustment".

Restriction

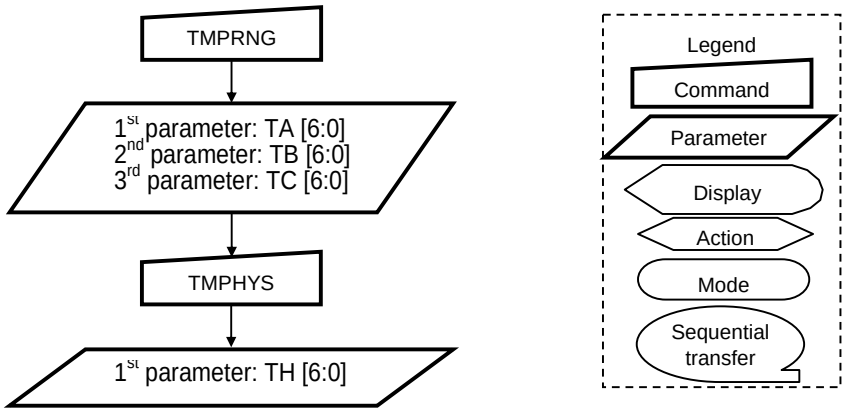
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	TA [6:0]	TB [6:0]	TC [6:0]
Power On Sequence	2Dh	7Fh	7Fh
S/W Reset	2Dh	7Fh	7Fh
H/W Reset	2Dh	7Fh	7Fh

Flow Chart



6.1.41 TMPHYS: Temperature Hysteresis Set for Frame Frequency Adjustment (B7h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	TMPHYS	0	↑	1	1	0	1	1	0	1	1	1	(B7h)
0	Parameter	1	↑	1	-	-	-	-	TH3	TH2	TH1	TH0	-

Description

Temperature hysteresis range set for frame frequency adjustment.

Parameter: Temperature hystetesis range set.

The relationship between temperature state and temperature range value is shown below.

TEMP Range Value	Temperature Rising State	Temperature Falling State
Frequency changing point A	TA [6:0] + TH [3:0]	TA [6:0]
Frequency changing point B	TB [6:0] + TH [3:0]	TB [6:0]
Frequency changing point C	TC [6:0] + TH [3:0]	TC [6:0]

NOTE: For the relationship between "Frequency changing point" and frame frequency, see section "5.11.9.3 Frame Frequency Adjustment".

Restriction

Temperature hysteresis value should be smaller than the gap of temperature range.

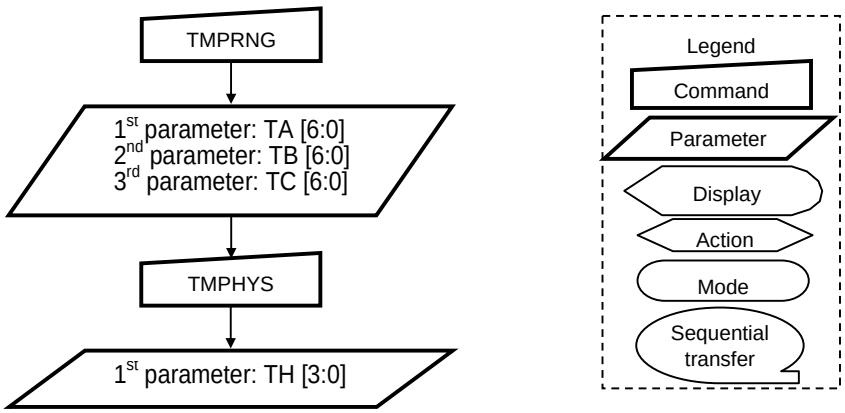
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	05h
S/W Reset	05h
H/W Reset	05h

Flow Chart



6.1.42 TMPREAD: Temperature Read-back (B8h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	TMPREAD	0	↑	1	1	0	1	1	1	0	0	0	(B8h)
0	Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
0	2nd parameter	1	1	↑	TBF	TD6	TD5	TD4	TD3	TD2	TD1	TD0	-

Description

Temperature read-back from the built-in temperature device.

The 1st parameter is dummy data

The 2nd parameter (TBF and TD6 to TD0): Temperature read busy and temperature value.

NOTE: For the relationship between TD [6:0] and temperature, see section "5.11.9 Temperature Compensation".

Restriction

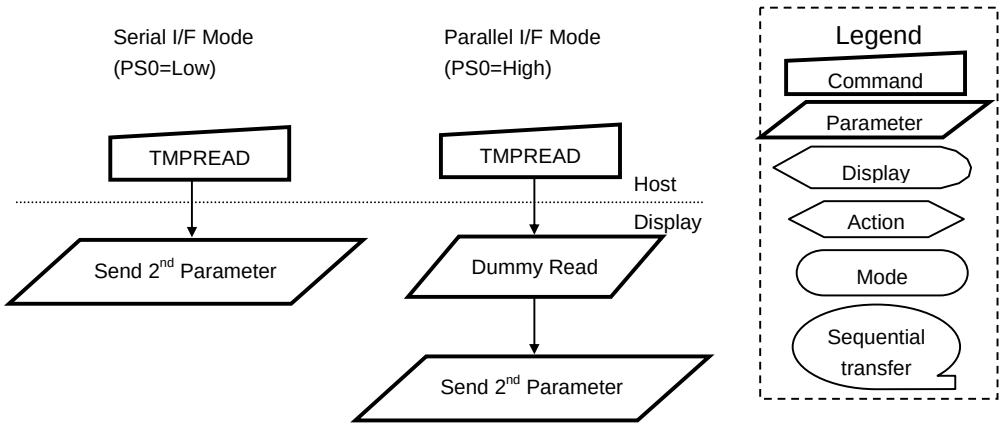
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	-
S/W Reset	-
H/W Reset	-

Flow Chart



6.1.43 DISCTR: Display Control (BAh)

Display timing related signal setup.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	DISCTR	0	↑	1	1	0	1	1	1	0	1	0	(BAh)
0	1st parameter	1	↑	1	-	-	-	-	-	FS2	FS1	FS0	-
0	2nd parameter	1	↑	1	-	-	-	FINV	NL3	NL2	NL1	NL0	-

Description

Display timing related signal set.

The 1st parameter is FI switching period

FS [2:0]	FI switching period
0	1 block (4-line)
1	2 block (8-line)
2	4 block (16-line)
3	6 block (24-line)
4	8 block (32-line)
5	10 block (40-line)
6	16 block (64-line)
7	Field

The 2nd parameter (FINV, NL[3:0]) :

FINV: Super-frame inversion set, NL [3:0]: N-block inversion

FINV	NL [3:0]	Inversely highlighted lines
1	0	Super-frame inversion
1	1	Super-frame inversion + 2 block (8-line)
1	2	Super-frame inversion + 3 block (12-line)
1	3	Super-frame inversion + 4 block (16-line)
:	:	:
1	15	Super-frame inversion + 16 block (64-line)
0	0	1 block (4-line)
0	1	2 block (8-line)
0	2	3 block (12-line)
0	3	4 block (16-line)
:	:	:
0	15	16 block (64-line)

Restriction

-

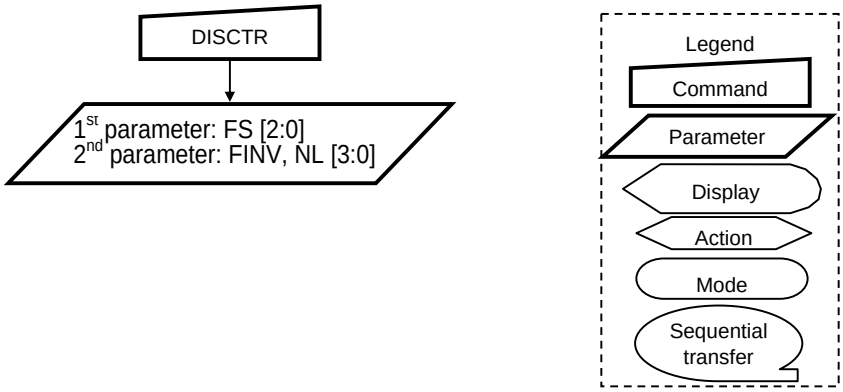
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	FS [2:0]	FINV	NL [3:0]
Power On Sequence	7h	1	5h
S/W Reset	7h	1	5h
H/W Reset	7h	1	5h

Flow Chart



6.1.44 EPVOL: Electrical Volume set for EEPROM (BBh)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	EPVOL	0	↑	1	1	0	1	1	1	0	1	1	(BBh)
0	1st parameter	1	↑	1	-	-	EOF5	EOF4	EOF3	EOF2	EOF1	EOF0	-
0	2nd parameter	1	↑	1	-	-	-	-	-	-	-	-	Dummy
0	3rd parameter	1	↑	1	-	-	-	-	-	ROF2	ROF1	ROF0	-

Description

Specify the voltage regulator circuit's electronic volume offset value (which will be stored in EEPROM).

The 1st parameter: Electrical Volume (EV) offset value.

EOF [5]	EOF [4:0]	Resultant Electrical Volume Value (EV_IN)
0	00h	EV_IN = EV + EOF[4:0] = EV + 0
0	01h	EV_IN = EV + EOF[4:0] = EV + 1
:	:	:
0	1Fh	EV_IN = EV + EOF[4:0] = EV + 31
1	00h	EV_IN = EV + EOF[4:0] = EV - 0
1	01h	EV_IN = EV + EOF[4:0] = EV - 1
:	:	:
1	1Fh	EV_IN = EV + EOF[4:0] = EV - 31

The 2nd parameter: Dummy byte.

The 3rd parameter: Resistance ratio (RR) offset value.

ROF [2]	ROF [1:0]	Resultant Resistance Ratio Value (RR_IN)	Default (RR=4)
0	0h	RR_IN = RR + ROF[1:0] = RR + 0	4
0	1h	RR_IN = RR + ROF[1:0] = RR + 1	5
0	2h	RR_IN = RR + ROF[1:0] = RR + 2	6
0	3h	RR_IN = RR + ROF[1:0] = RR + 3	7
1	0h	RR_IN = RR + ROF[1:0] = RR - 0	4
1	1h	RR_IN = RR + ROF[1:0] = RR - 1	3
1	2h	RR_IN = RR + ROF[1:0] = RR - 2	2
1	3h	RR_IN = RR + ROF[1:0] = RR - 3	1

NOTE: If EV_IN < 0, EV_IN becomes 0, and if EV_IN ≥ 127, EV_IN value becomes 127.

If RR_IN < 0, RR_IN becomes 0, and if RR_IN ≥ 7, RR_IN value becomes 7.

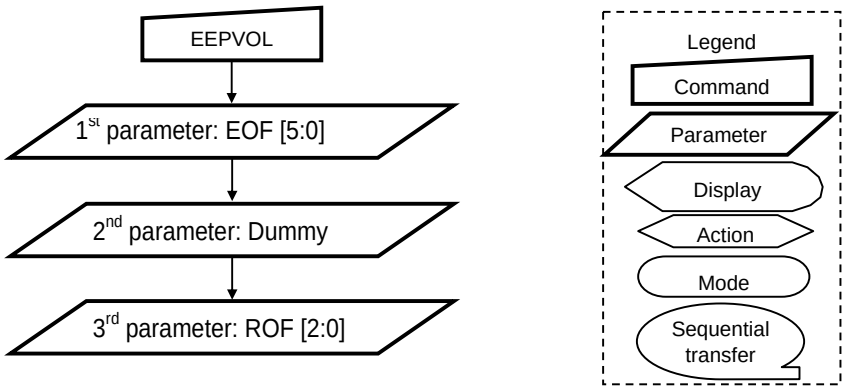
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	-
S/W Reset	-
H/W Reset	-

Flow Chart	

EEPVOL
1st parameter: EOF [5:0]
2nd parameter: Dummy
3rd parameter: ROF [2:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.1.45 EPWROUT: EEPROM Write Out (D0h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	EPWROUT	0	↑	1	1	1	0	1	0	0	0	0	(D0h)
0	Parameter	No Parameter											

Description	EEPROM write mode disable.
Restriction	It will be necessary to wait more than 100msec after EEPROM write mode start (EPWRIN).

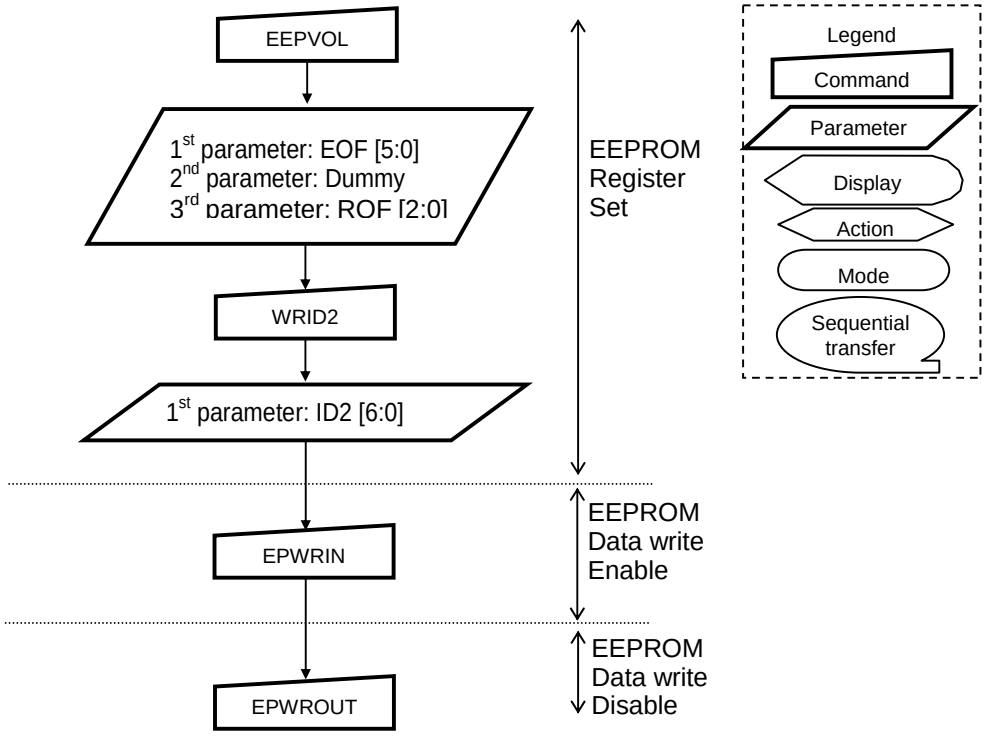
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	No
Normal Mode On, Idle Mode On, Sleep Out	No
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	EEPROM write out
S/W Reset	EEPROM write out
H/W Reset	EEPROM write out

Flow Chart



6.1.46 EPWRIN: EEPROM Write In (D1h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	EPWRIN	0	↑	1	1	1	0	1	0	0	0	1	(D1h)
0	Parameter	No Parameter											

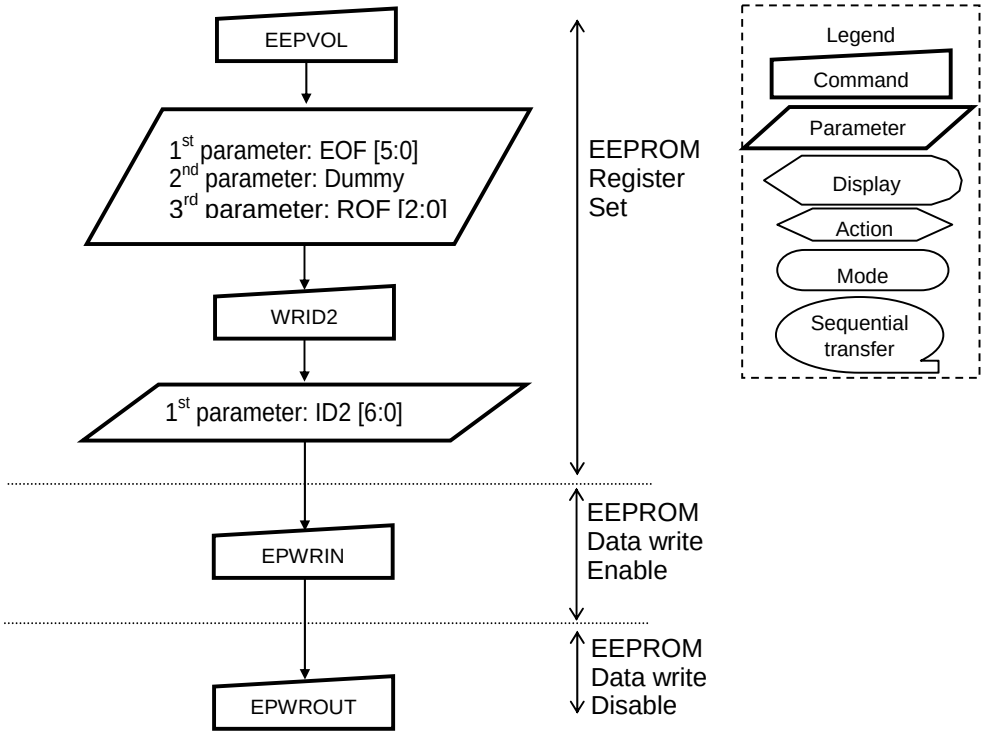
Description	EEPROM write mode start.
Restriction	Before EPWRIN command, EOF [5:0] and ROF [2:0] parameter of EEPVOL command and ID2 [6:0] of WRID2 command need to be pre-set. And it will be necessary to wait more than 1.5sec before exiting EEPROM write mode (EPWROUT).
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	No
Normal Mode On, Idle Mode On, Sleep Out	No
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	**Yes**

Default

Status	Default Value
Power On Sequence	EEPROM write out
S/W Reset	EEPROM write out
H/W Reset	EEPROM write out

Flow Chart



6.1.47 RDEV: Read Electrical Volume Value (3Fh)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	RDEV	0	↑	1	1	1	0	1	0	1	0	0	(D4h)
0	Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
0	2nd parameter	1	1	↑	-	EV6	EV5	EV4	EV3	EV2	EV1	EV0	-

Description

This read byte returns 7-bit Electrical Volume Value.
The 1st parameter is dummy data
The 2nd parameter (EV6 to EV0): Internal Electrical Volume Value.

Restriction

-

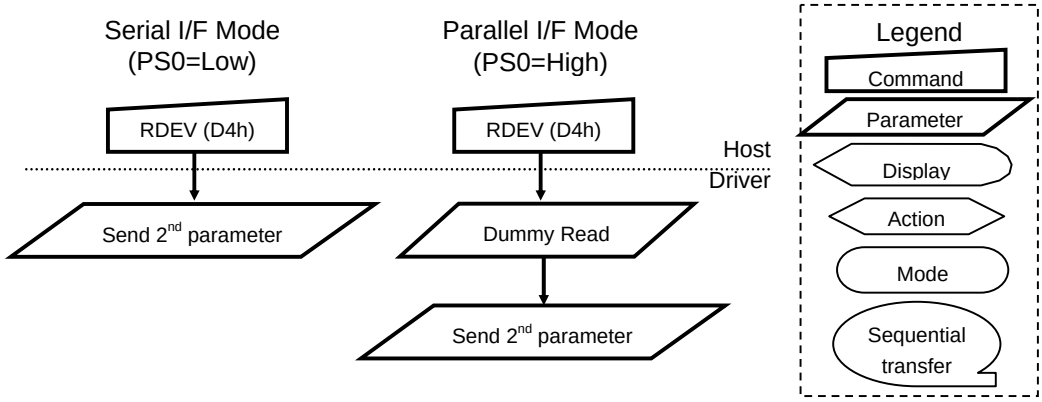
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	3Fh
S/W Reset	3Fh
H/W Reset	3Fh

Flow Chart



6.1.48 RDRR: Read Resistor Ratio Value (D5h)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	RDRR	0	↑	1	1	1	0	1	0	1	0	1	(D5h)
0	Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
0	2nd parameter	1	1	↑	-	-	-	-	-	RR2	RR1	RR0	-

Description

This read byte returns 3-bit Resistor Ratio Value.
The 1st parameter is dummy data
The 2nd parameter (RR2 to RR0): Internal Resistor Ratio Value.

Restriction

-

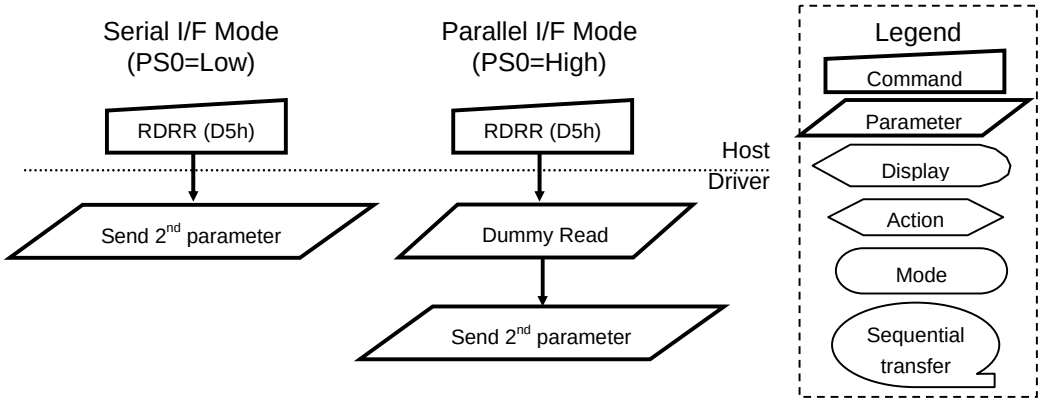
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	04h
S/W Reset	04h
H/W Reset	04h

Flow Chart



6.1.49 TEST1: Test Command1 (E-h)

This instruction is a testing instruction code for Leadis. Please do not use it.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	TEST1	0	↑	1	1	1	1	0	-	-	-	-	(E-h)

6.1.50 TEST2: Test Command2 (F-h)

This instruction is a testing instruction code for Leadis. Please do not use it.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
0	TEST2	0	↑	1	1	1	1	1	-	-	-	-	(F-h)

6.2 INSTRUCTION CODE 1 (ISS=1)

6.2.1 Instruction Code Table

Table 6.2.1 Instruction Code1 (ISS=1)

"-": Don't care

Instruction	Refer	ISS	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)	Function
NOP	6.2.2	1	0	↑	1	0	0	1	0	0	1	0	1	**(25h)**	No operation
OSCON	6.2.3	1	0	↑	1	1	1	0	1	0	0	0	1	**(D1h)**	Oscillator on
OSCOFF	6.2.4	1	0	↑	1	1	1	0	1	0	0	1	0	**(D2h)**	Oscillator off
BSTRON	6.2.5	1	0	↑	1	0	0	1	0	0	0	0	0	**(20h)**	All power on
BSTROFF	6.2.6	1	0	↑	1	0	0	1	0	0	0	0	1	**(21h)**	All power off
SLPIN	6.2.7	1	0	↑	1	1	0	0	1	0	1	0	1	**(95h)**	Sleep in
SLPOUT	6.2.8	1	0	↑	1	1	0	0	1	0	1	0	0	**(94h)**	Sleep out
PTLOUT	6.2.9	1	0	↑	1	1	0	1	0	1	0	0	1	**(A9h)**	Partial display off
PTLIN	6.2.10	1	0	↑	1	1	0	1	0	1	0	0	0	**(A8h)**	Partial area set & on
		1	1	↑	1	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-	Partial start line address
		1	1	↑	1	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	-	Partial end line address
DISNOR	6.2.11	1	1	↑	1	1	0	1	0	0	1	1	0	**(A6h)**	Display inversion off (normal)
DISINV	6.2.12	1	1	↑	1	1	0	1	0	0	1	1	1	**(A7h)**	Display inversion on
DISPOFF	6.2.13	1	1	↑	1	1	0	1	0	1	1	1	0	**(AEh)**	Display off
DISPON	6.2.14	1	1	↑	1	1	0	1	0	1	1	1	1	**(AFh)**	Display on
CASET	6.2.15	1	0	↑	1	0	0	0	1	0	1	0	1	**(15h)**	Column address set
		1	1	↑	1	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	-	X_ADR start: 0 ≤ XS ≤ 83h
		1	1	↑	1	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	-	X_ADR end: XS ≤ XE ≤ 83h
RASET	6.2.16	1	0	↑	1	0	1	1	1	0	1	0	1	**(75h)**	Row address set
		1	1	↑	1	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	-	Y_ADR start: 0 ≤ YS ≤ 83h
		1	1	↑	1	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	-	Y_ADR end: YS ≤ YE ≤ 83h
RAMWR	6.2.17	1	0	↑	1	0	1	0	1	1	1	0	0	**(5Ch)**	Memory write
		1	1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	-	Write data
RAMRD	6.2.18	1	0	↑	1	0	1	0	1	1	1	0	1	**(5Dh)**	Memory Read
		1	1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	1	↑	D7	D6	D5	D4	D3	D2	D1	D0	-	Read data
RGBSET	6.2.19	1	0	↑	1	1	1	0	0	1	1	1	0	**(CEh)**	Color set for 256 color display
		1	1	↑	1	-	-	-	-	R3	R2	R1	R0	-	Red tone (000)
		1	1	↑	1	:	:	:	:	:	:	:	:	:	:
		1	1	↑	1	-	-	-	-	R3	R2	R1	R0	-	Red tone (111)
		1	1	↑	1	-	-	-	-	G3	G2	G1	G0	-	Green tone (000)
		1	1	↑	1	:	:	:	:	:	:	:	:	:	:
		1	1	↑	1	-	-	-	-	G3	G2	G1	G0	-	Green tone (111)
		1	1	↑	1	-	-	-	-	B3	B2	B1	B0	-	Blue tone (00)
		1	1	↑	1	:	:	:	:	:	:	:	:	:	:
		1	1	↑	1	-	-	-	-	B3	B2	B1	B0	-	Blue tone (11)
ASCSET	6.2.20	1	0	↑	1	1	0	1	0	1	0	1	0	**(AAh)**	Scroll area set
		1	1	↑	1	SSL7	SSL6	SSL5	SSL4	SSL3	SSL2	SSL1	SSL0	-	Scroll start line
		1	1	↑	1	SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0	-	Scroll end line
		1	1	↑	1	SFL7	SFL6	SFL5	SFL4	SFL3	SFL2	SFL1	SF0	-	Scroll specified line
		1	1	↑	1	-	-	-	-	-	-	SMD1	SMD0	-	Area scroll mode
VSCSAD	6.2.21	1	0	↑	1	1	0	1	0	1	0	1	1	**(ABh)**	Scroll start address set
		1	1	↑	1	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	-	Start scroll line address of RAM

Table 6.2.2 Instruction Code1 (ISS=1, Continued)

"-": Don't care

Instruction	Refer	ISS	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)	Function
DATCTR	6.2.22	1	0	↑	1	1	0	1	1	1	1	0	0	**(BCh)**	Data control
		1	1	↑	1	-	-	-	-	-	MV	MX	MY	-	Row/column address control
		1	1	↑	1	-	-	-	-	-	-	-	RGB	-	RGB
		1	1	↑	1	-	-	-	-	-	GS2	GS1	GS0	-	Gray-scale setup
RMWIN	6.2.23	1	0	↑	1	1	1	1	0	0	0	0	0	**(E0h)**	Read & modify write on
RMWOUT	6.2.24	1	0	↑	1	1	1	1	0	1	1	1	0	**(EEh)**	Read & modify write off
VOLCTR	6.2.25	1	0	↑	1	1	0	0	0	0	0	0	1	**(81h)**	Electronic volume control
		1	1	↑	1	-	EV6	EV5	EV4	EV3	EV2	EV1	EV0	-	VXH2 volume value
		1	1	↑	1	-	-	-	-	-	RR2	RR1	RR0	-	Resistance ratio set
VOLUP	6.2.26	1	0	↑	1	1	1	0	1	0	1	1	0	**(D6h)**	EV increment
VOLDOWN	6.2.27	1	0	↑	1	1	1	0	1	0	1	1	1	**(D7h)**	EV decrement
DISCTR	6.2.28	1	0	↑	1	1	0	1	1	1	0	1	0	**(BAh)**	Display control
		1	1	↑	1	-	-	-	-	-	FS2	FS1	FS0	-	F1/F2 pattern
		1	1	↑	1	-	-	-	FINV	NL3	NL2	NL1	NL0	-	FR inversion-set value
FRMSEL	6.2.29	1	0	↑	1	1	0	1	1	0	1	0	0	**(B4h)**	Frame frequency select
		1	1	↑	1	-	-	-	FA4	FA3	FA2	FA1	FA0	-	Frame frequency in Temp range A
		1	1	↑	1	-	-	-	FB4	FB3	FB2	FB1	FB0	-	Frame frequency in Temp range B
		1	1	↑	1	-	-	-	FC4	FC3	FC2	FC1	FC0	-	Frame frequency in Temp range C
		1	1	↑	1	-	-	-	FD4	FD3	FD2	FD1	FD0	-	Frame frequency in Temp range D
FRM8SEL	6.2.30	1	0	↑	1	1	0	1	1	0	1	0	1	**(B5h)**	Frame frequency select (8-color)
		1	1	↑	1	-	-	-	F8A4	F8A3	F8A2	F8A1	F8A0	-	Frame frequency in Temp range A
		1	1	↑	1	-	-	-	F8B4	F8B3	F8B2	F8B1	F8B0	-	Frame frequency in Temp range B
		1	1	↑	1	-	-	-	F8C4	F8C3	F8C2	F8C1	F8C0	-	Frame frequency in Temp range C
		1	1	↑	1	-	-	-	F8D4	F8D3	F8D2	F8D1	F8D0	-	Frame frequency in Temp range D
TMPRNG	6.2.31	1	0	↑	1	1	0	1	1	0	1	1	0	**(B6h)**	Temp range set
		1	1	↑	1	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	-	Temp range A
		1	1	↑	1	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	-	Temp range B
		1	1	↑	1	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	-	Temp range C
TMPHIS	6.2.32	1	0	↑	1	1	0	1	1	0	1	1	1	**(B7h)**	Temp hysteresis range set
		1	1	↑	1	-	-	-	-	TH3	TH2	TH1	TH0	-	Hysteresis value set
TMPREAD	6.2.33	1	0	↑	1	1	0	1	1	1	0	0	0	**(B8h)**	Temperature read back
		1	1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	1	↑	BF	T6	T5	T4	T3	T2	T1	T0	-	Read parameter
EPVOL	6.2.34	1	0	↑	1	1	1	0	0	0	0	0	0	**(C0h)**	Electronic volume offset
		1	1	↑	1	-	-	EOF5	EOF4	EOF3	EOF2	EOF1	EOF0	-	EV offset
		1	1	↑	1	-	-	-	-	-	-	-	-	-	Dummy byte
		1	1	↑	1	-	-	-	-	-	ROF2	ROF1	ROF0	-	RR offset
EPWRIN	6.2.35	1	0	↑	1	1	1	0	0	1	1	0	1	**(CDh)**	EEPROM write start
EPWROUT	6.2.36	1	0	↑	1	1	1	0	0	1	1	0	0	**(CCh)**	EEPROM write end
RDEV	6.2.37	1	0	↑	1	0	1	1	1	1	1	0	0	**(7Ch)**	Read internal contrast (EV_IN)
		1	1	1	↑	-	-	-	-	-	-	-	-	**-**	Dummy read
		1	1	1	↑	-	EV6	EV5	EV4	EV3	EV2	EV1	EV0	**-**	Read parameter
RDRR	6.2.38	1	0	↑	1	0	1	1	1	1	1	0	1	**(7Dh)**	Read internal resistor ratio (RR_IN)
		1	1	1	↑	-	-	-	-	-	-	-	-	**-**	Dummy read
		1	1	1	↑	-	-	-	-	-	RR2	RR1	RR0	**-**	Read parameter

Table 6.2.3 Instruction Code1 (ISS=1, Continued)

"-": Don't care

Instruction	Refer	ISS	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code) Default	Function
RDID1	6.2.39	1	0	↑	1	0	0	1	0	1	0	1	0	**(DAh)**	Read ID1
		1	1	1	↑	-	-	-	-	-	-	-	-	**-**	Dummy read
		1	1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-	Read parameter
RDID2	6.2.40	1	0	↑	1	0	0	1	0	1	0	1	1	**(DBh)**	Read ID2
		1	1	1	↑	-	-	-	-	-	-	-	-	**-**	Dummy read
		1	1	1	↑	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-	Read parameter
RDID3	6.2.41	1	0	↑	1	0	0	1	0	1	1	0	0	**(DCh)**	Read ID2
		1	1	1	↑	-	-	-	-	-	-	-	-	**-**	Dummy read
		1	1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-	Read parameter
IDMOFF	6.2.42	1	0	↑	1	0	0	1	1	1	0	0	0	**(38h)**	Idle mode off
IDMON	6.2.43	1	0	↑	1	0	0	1	1	1	0	0	1	**(39h)**	Idle mode on
TEOFF	6.2.44	1	0	↑	1	0	0	1	1	0	1	0	0	**(34h)**	Tearing effect line off
TEON	6.2.45	1	0	↑	1	0	0	1	1	0	1	0	1	**(35h)**	Tearing effect line on
TEST1	6.2.46	1	0	↑	1	0	1	1	0	-	-	-	-	**(6-h)**	Test command1
TEST2	6.2.47	1	0	↑	1	0	0	0	0	-	-	-	-	**(0-h)**	Test command2

NOTE:

1) After the H/W reset by !RES pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section)

2) Undefined commands are treated as NOP (00 h) command.

6.2.2 NOP (25h)

No operation. This command can be used to interrupt an on-going instruction.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	NOP	0	↑	1	0	0	1	0	0	1	0	1	(25h)
1	Parameter	No Parameter											

6.2.3 OSCON: Oscillator On (D1h)

Turn on the internal oscillator circuit.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	OSCON	0	↑	1	1	1	0	1	0	0	0	1	(D1h)
1	Parameter	No Parameter											

6.2.4 OSCOFF: Oscillator Off (D2h)

Turn off the internal oscillator circuit.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	OSCOFF	0	↑	1	1	1	0	1	0	0	1	0	(D2h)
1	Parameter	No Parameter											

6.2.5 BSTRON: Power All On (20h)

Turn on all the internal power circuit.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	BSTRON	0	↑	1	0	0	1	0	0	0	0	0	(20h)
1	Parameter	No Parameter											

6.2.6 BSTROFF: Power All Off (21h)

Turn on all the internal power circuit.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	BSTROFF	0	↑	1	0	0	1	0	0	0	0	1	(21h)
1	Parameter	No Parameter											

6.2.7 SLPIN: Sleep In (95h)

Enter power down mode, sleep mode. In the sleep mode output voltages of all LCD driver pins are ground, the DC-DC converters and oscillator are switched off. Before using sleep in command, it is necessary to turn off the display by entering the display off command.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	SLPIN	0	↑	1	1	0	0	1	0	1	0	1	(95h)
1	Parameter	No Parameter											

6.2.8 SLPOUT: Sleep Out (94h)

Switching off sleep IN mode. When leaving the sleep IN mode, it might be necessary to wait for a certain time before the power circuits become stable.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	SLPOUT	0	↑	1	1	0	0	1	0	1	0	0	(94h)
1	Parameter	No Parameter											

6.2.9 PTLOUT: Partial Display Mode Off (A9h)

Exit partial display mode.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	PTLOUT	0	↑	1	1	0	1	0	1	0	0	1	(A9h)
1	Parameter	No Parameter											

6.2.10 PTLIN: Partial Area Set & Partial Display Mode On (A8h)

The partial area command sets the partial display area and display the RAM content of these area. In partial display mode the driving voltage and frame frequency are same as the normal display mode but the current consumption is reduced.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	PTLIN	0	↑	1	1	0	1	0	1	0	0	0	(A8h)
1	1st parameter	1	↑	1	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-
1	2nd parameter	1	↑	1	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	-

The following steps must be performed to enter partial mode:
- Set partial start line address PSL [7:0]
- Set partial end line address PEL [7:0]

When Setting the addresses the following conditions must be ensured:
$0 \le PSL \le 131$, $0 \le PEL \le 131$

During partial display mode, display window are divided as displaying area and non-displaying area, and in the non-displaying area COM outputs become VC and SEG outputs become VXH1 or VXL1 according to the internal alternating signal.

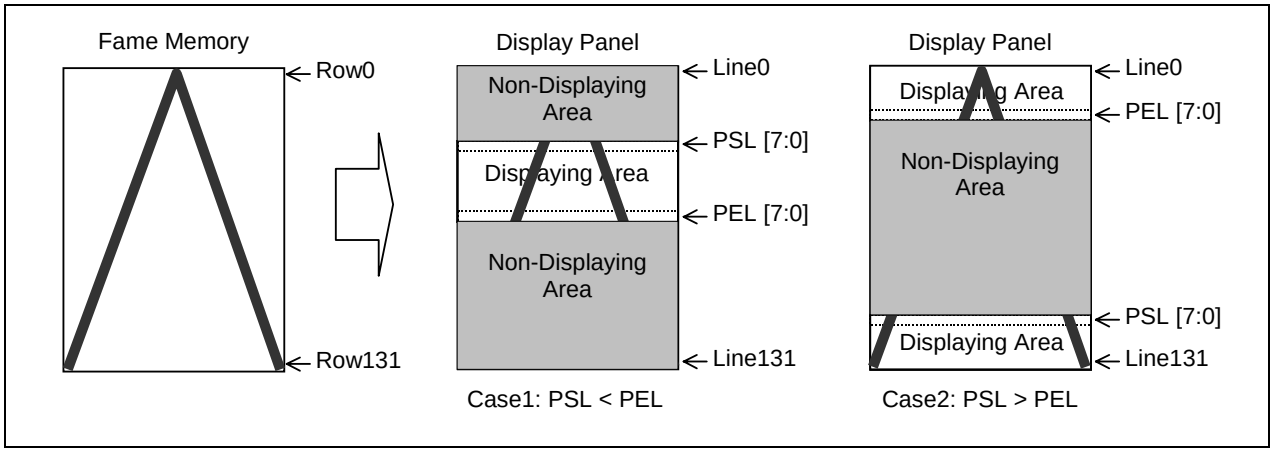


Fig. 6.2.1 Partial display mode

6.2.11 DISNOR: Normal Display Mode (Inversion Off) (A6h)

Turns the display into a normal screen without modifying the display data RAM.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	INVOFF	0	↑	1	1	0	1	0	0	1	1	0	(A6h)
1	Parameter	No Parameter											

6.2.12 DISINV: Display Inversion On (A7h)

Turns the display into a inverted screen without modifying the display data RAM.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	INVON	0	↑	1	1	0	1	0	0	1	1	1	(A7h)
1	Parameter	No Parameter											

6.2.13 DISPOFF: Display Off (AEh)

Turn off the display as of the blank screen with no regard to the display data RAM.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	DISPOFF	0	↑	1	1	0	1	0	1	1	1	0	(AEh)
1	Parameter	No Parameter											

6.2.14 DISPON: Display On (AFh)

Turn on the display screen according to the current display data RAM content and the display timing and setting.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	DISPON	0	↑	1	1	0	1	0	1	1	1	1	(AFh)
1	Parameter	No Parameter											

6.2.15 CASET: Column Address Set (15h)

The display data RAM parameters XS and XE define the column address range of the display data RAM, for writing data. The XS and XE are defined between 0 and 131 (83hex) and XS must be smaller then XE.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	CASET	0	↑	1	0	0	0	1	0	1	0	1	(15h)
1	1st parameter	1	↑	1	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	00h
1	2nd parameter	1	↑	1	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	81h

6.2.16 RASET: Row Address Set (75h)

The display data RAM parameters YS and YE define the row address range of the display data RAM, for writing data. The YS and YE are defined between 0 and 131 (83hex) and YS must be smaller then YE.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	RASET	0	↑	1	0	1	1	1	0	1	0	1	(75h)
1	1st parameter	1	↑	1	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	02h
1	2nd parameter	1	↑	1	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	83h

6.2.17 RAMWR: Memory Write (5Ch)

Data written to the display memory (RAM) is validated by this command. Entering this command always returns the row address and column address to the start address. Contents of the display data RAM is written by the data entered following this command and at the same time the row address or column address is incremented. The data write mode turned on by this command can be automatically cancelled by entering another command.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	RAMWR	0	↑	1	0	1	0	1	1	1	0	0	(5Ch)
1	Data write	1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	-
:	:	:	:	:	:	:	:	:	:	:	:	:	:
1	Data write	1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	-

6.2.18 RAMRD: Memory Read (5Dh)

Data read from the display memory (RAM) is validated by this command. Entering this command always returns the row address and column address to the start address. Contents of the display data RAM is read via the D7 to D0 pad following this command and at the same time the row address or column address is incremented. The data read mode turned on by this command can be automatically cancelled by entering another command.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	RAMRD	0	↑	1	0	1	0	1	1	1	0	1	(5Dh)
1	Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
1	Data read	1	1	↑	D7	D6	D5	D4	D3	D2	D1	D0	-
:	:	:	:	:	:	:	:	:	:	:	:	:	:
1	Data read	1	1	↑	D7	D6	D5	D4	D3	D2	D1	D0	-

6.2.19 RGBSET: Colour Set for 256-Color Display (CEh)

With this command a mapping from 256 color or 4k-color to the 65k-color RAM of the LDS176 is done.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	RGBSET	0	↑	1	1	1	0	0	1	1	1	0	(CEh)
1	1st parameter	1	↑	1	-	-	-	-	R03	R02	R01	R00	00h
1	:	1	↑	1	-	-	-	-	Rn3	Rn2	Rn1	Rn0	00h
1	8th parameter	1	↑	1	-	-	-	-	R73	R72	R71	R70	00h
1	9th parameter	1	↑	1	-	-	-	-	G03	G02	G01	G00	00h
1	:	1	↑	1	-	-	-	-	Gn3	Gn2	Gn1	Gn0	00h
1	16th parameter	1	↑	1	-	-	-	-	G73	G72	G71	G70	00h
1	17th parameter	1	↑	1	-	-	-	-	B03	B02	B01	B00	00h
1	:	1	↑	1	-	-	-	-	Bn3	Bn2	Bn1	Bn0	00h
1	20th parameter	1	↑	1	-	-	-	-	B33	B32	B31	B30	00h

This command is used to define the LUT for 8bit-to-12bit color depth conversations. (See Also Table 5.2.3)
20 Bytes must be written to the LUT regardless of the color mode. Only the values in Section 5.2.6 are referred.
This command has no effect on other commands/parameters and Contents of frame memory.
Visible change takes effect next time the Frame Memory is written to.

6.2.20 ASCSET: Scroll Area Set (AAh)

The scroll area command sets the scroll display area and display the RAM content of these area. By using VSCSAD (Vertical Scroll Start Address) command, the display data within scroll area can be scrolled up and down.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	ASCSET	0	↑	1	1	0	1	0	1	0	1	0	(AAh)
1	1st parameter	1	↑	1	SSL7	SSL6	SSL5	SSL4	SSL3	SSL2	SSL1	SSL0	-
1	2nd parameter	1	↑	1	SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0	-
1	3rd parameter	1	↑	1	SFL7	SFL6	SFL5	SFL4	SFL3	SFL2	SFL1	SFL0	-
1	4th parameter	1	↑	1	-	-	-	-	-	-	SMD1	SMD0	-

In table below the used parameters are explained with their reset states (see also ***Fig. 6.2.2***).

Parameter	Description	Reset state
SSL [7:0]	Top scroll line address	00h
SEL [7:0]	Bottom scroll line address	00h
SFL [7:0]	Number of scroll specified line	00h
SMD [1:0]	Scroll mode	3

SMD [1:0]: Scroll mode set parameter (see also ***Fig. 6.2.3***).

SMD1	SMD0	Scroll Mode	Scroll area set register change		
			SSL [7:0]	SEL [7:0]	SFL [7:0]
0	0	Center screen scroll mode	No change	No change	No change
0	1	Top screen scroll mode	**00h**	No change	No change
1	0	Bottom screen scroll mode	No change	**83h**	**SEL [7:0]**
1	1	Whole screen scroll mode	**00h**	**83h**	**SEL [7:0]**

6.2.21 VSCSAD: Vertical Scroll Start Address of RAM (ABh)

Scroll start address set.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	VSCSAD	0	↑	1	1	0	1	0	1	0	1	1	(ABh)
1	Parameter	1	↑	1	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	-

NOTE: Scroll start address should be in scroll area (should not be in top or bottom fixed area).

The following steps must be performed to enter scroll mode:

Define the scroll area
- Set scroll start block: SSL [7:0]
- Set scroll end block: SEL [7:0]
- Set scroll specified block: SFL [7:0]
- Set scroll mode: SMD [1:0]

Vertical scroll start address set: SSA [7:0]

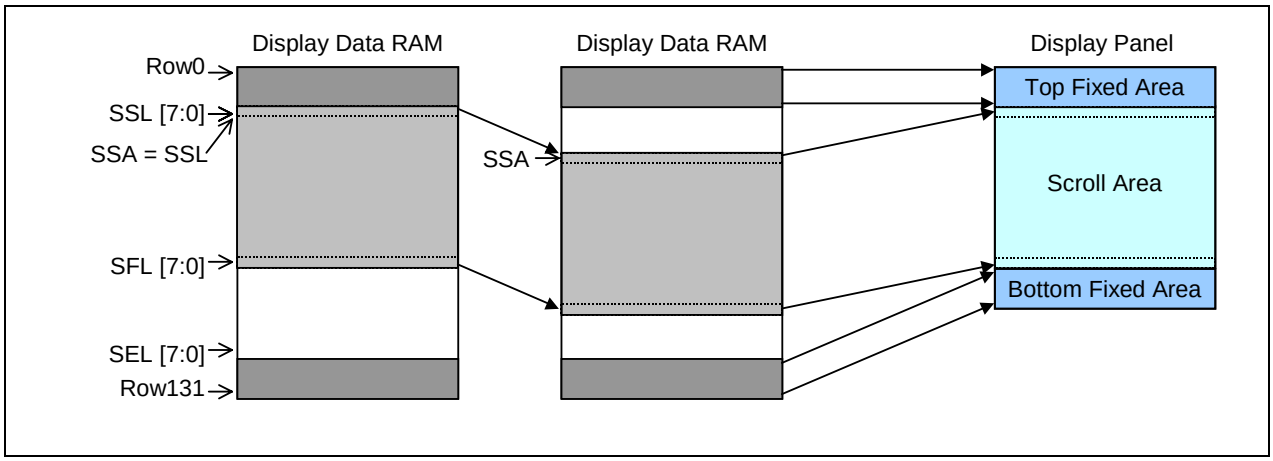


Fig. 6.2.2 Vertical scroll & display window partition

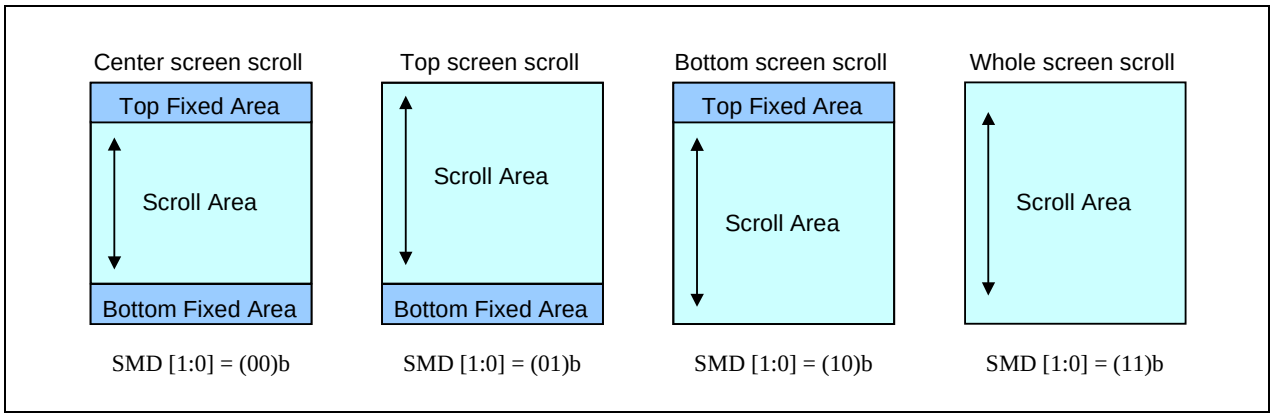


Fig. 6.2.3 Vertical scroll mode according to the SMD [1:0] value

6.2.22 DATCTR: Data Access Control (BCh)

The display data RAM access conditions RAM can be defined using the following command.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	DATCTR	0	↑	1	1	0	1	1	1	1	0	0	(BCh)
1	1st parameter	1	↑	1	-	-	-	-	-	MV	MX	MY	-
1	2nd parameter	1	↑	1	-	-	-	-	-	-	-	RGB	-
1	3rd parameter	1	↑	1	-	-	-	-	-	GS2	GS1	GS0	-

In table below the used single control bits are explained with their reset states.

Parameter	0 (Reset state)	1
MY	No mirror Y	Mirror Y
MX	No mirror X	Mirror X
MV	RAM write in X direction	RAM write in Y direction
RGB	RGB order	BGR order

GS [2:0]: Gray-scale number set parameter

GS2	GS1	GS0	Description
0	0	1	256 Color
0	1	0	4k Color type A
1	0	0	4k Color type B
1	0	1	65k Color

6.2.23 RMWIN: Read Modify Write In (E0h)

Modify read mode on command.
This instruction stops the automatic increment of the column address by the read display data operation, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	RMWIN	0	↑	1	1	1	1	0	0	0	0	0	(E0h)
1	Parameter	No Parameter											

6.2.24 RMWOUT: Read Modify Write Out (EEh)

Modify read mode off command.
Modify read mode is disables and column row address returns to the initial value just before the RMWIN command.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	RMWOUT	0	↑	1	1	1	1	0	1	1	1	0	(EEh)
1	Parameter	No Parameter											

6.2.25 VOLCTR: Electrical Volume Control (81h)

Specify the voltage regulator circuit's electronic volume value α and resistance ratio of built-in voltage regulating resistor.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	VOLCTR	0	↑	1	1	0	0	0	0	0	0	1	(81h)
1	1st parameter	1	↑	1	-	EV6	EV5	EV4	EV3	EV2	EV1	EV0	-
1	2nd parameter	1	↑	1	-	-	-	-	-	RR2	RR1	RR0	-

EV [6:0]: Specify VXH2 electronic volume value.
RR [2:0]: Specify resistance ratio of the internal resistor.

6.2.26 VOLUP: Electrical Volume Increment (D6h)

This command increases electronic volume value EV [6:0] by 1. If the value is set to 7F (hex), after this command, the value wrap to 0.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	VOLUP	0	↑	1	1	1	0	1	0	1	1	0	(D6h)
1	Parameter	No Parameter											

6.2.27 VOLDOWN: Electrical Volume Decrement (D7h)

This command decreases electronic volume value EV [6:0] by 1. If the value is set to 0 (hex), after this command, the value wrap to 7F (hex).

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	VOLDOWN	0	↑	1	1	1	0	1	0	1	1	1	(D7h)
1	Parameter	No Parameter											

6.2.28 DISCTR: Display Control (BAh)

Display timing related signal setup.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	DISCTR	0	↑	1	1	0	1	1	1	0	1	0	(BAh)
1	1st parameter	1	↑	1	-	-	-	-	-	FS2	FS1	FS0	-
1	2nd parameter	1	↑	1	-	-	-	FINV	NL3	NL2	NL1	NL0	-

The 1st parameter is FI switching period

FS [2:0]	FI switching period
0	1 block (4-line)
1	2 block (8-line)
2	4 block (16-line)
3	6 block (24-line)
4	8 block (32-line)
5	10 block (40-line)
6	16 block (64-line)
7	Field

The 2nd parameter (FINV, NL [3:0]):

FINV: Super-frame inversion set, NL [3:0]: N-block inversion

FINV	NL [3:0]	Inversely highlighted lines
1	0	Super-frame inversion
1	1	Super-frame inversion + 2 block (8-line)
1	2	Super-frame inversion + 3 block (12-line)
1	3	Super-frame inversion + 4 block (16-line)
:	:	:
1	15	Super-frame inversion + 16 block (64-line)
0	0	1 block (4-line)
0	1	2 block (8-line)
0	2	3 block (12-line)
0	3	4 block (16-line)
:	:	:
0	15	16 block (64-line)

6.2.29 FRMSEL: Frame frequency in normal mode (B4h)

Select frame frequency in normal display mode.
1st parameter: Frame frequency value set in TEMP range 0(–35°C) to TA
2nd parameter: Frame frequency value set in TEMP range TA to TB
3rd parameter: Frame frequency value set in TEMP range TB to TC
4th parameter: Frame frequency value set in TEMP range TC to 127(92°C)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	FRMSEL	0	↑	1	1	0	1	1	0	1	0	0	(B4h)
1	1st parameter	1	↑	1	-	-	-	FA4	FA3	FA2	FA1	FA0	-
1	2nd parameter	1	↑	1	-	-	-	FB4	FB3	FB2	FB1	FB0	-
1	3rd parameter	1	↑	1	-	-	-	FC4	FC3	FC2	FC1	FC0	-
1	4th parameter	1	↑	1	-	-	-	FD4	FD3	FD2	FD1	FD0	-

*NOTE: For the relationship between FA[5:0] ~ FD[5:0] and frame frequency, see "**Table 6.1.4**"*
*For more detail about frequency adjustment method, see section "*5.11.9.3 Frame Frequency Adjustment*".*

6.2.30 FRM8SEL: Frame frequency in idle mode (8-color mode) (B5h)

Select frame frequency in normal display mode.
1st parameter: Frame frequency value set in TEMP range 0(–35°C) to TA
2nd parameter: Frame frequency value set in TEMP range TA to TB
3rd parameter: Frame frequency value set in TEMP range TB to TC
4th parameter: Frame frequency value set in TEMP range TC to 127(92°C)

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	FRM8SEL	0	↑	1	1	0	1	1	0	1	0	1	(B5h)
1	1st parameter	1	↑	1	-	-	-	F8A4	F8A3	F8A2	F8A1	F8A0	-
1	2nd parameter	1	↑	1	-	-	-	F8B4	F8B3	F8B2	F8B1	F8B0	-
1	3rd parameter	1	↑	1	-	-	-	F8C4	F8C3	F8C2	F8C1	F8C0	-
1	4th parameter	1	↑	1	-	-	-	F8D4	F8D3	F8D2	F8D1	F8D0	-

*NOTE: For the relationship between F8A[5:0] ~ F8D[5:0] and frame frequency, see "**Table 6.1.4**"*
*For more detail about frequency adjustment method, see section "*5.11.9.3 Frame Frequency Adjustment*".*

6.2.31 TMPRNG: Temperature Range Set for Frame Frequency Adjustment (B6h)

Temperature range set for automatic frame frequency adjustment operation according the current temperature value.
1st parameter: Temperature range A value set
2nd parameter: Temperature range B value set
3rd parameter: Temperature range C value set

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	TMPRNG	0	↑	1	1	0	1	1	0	1	1	0	(B6h)
1	1st parameter	1	↑	1	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	-
1	2nd parameter	1	↑	1	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	-
1	3rd parameter	1	↑	1	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	-

*NOTE: For the relationship between TA[6:0] to TC[6:0] and frame frequency, see section "*5.11.9.3 Frame Frequency Adjustment*".*

6.2.32 TMPHYS: Temperature Hysteresis Set for Frame Frequency Adjustment (B7h)

Temperature hysteresis range set for frame frequency adjustment.
Parameter: Temperature hystetesis range set.
Temperature hysteresis value should be smaller than the gap of temperature range.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	TMPHYS	0	↑	1	1	0	1	1	0	1	1	1	(B7h)
1	Parameter	1	↑	1	-	-	-	-	TH3	TH2	TH1	TH0	-

The relationship between temperature state and temperature range value is shown below.

TEMP Range Value	Temperature Rising	Temperature Falling
Frequency changing point A	TA [6:0] + TH [3:0]	TA [6:0]
Frequency changing point B	TB [6:0] + TH [3:0]	TB [6:0]
Frequency changing point C	TC [6:0] + TH [3:0]	TC [6:0]

NOTE: For the relationship between "Frequency changing point" and frame frequency, see section "5.11.9.3 Frame Frequency Adjustment".

6.2.33 TMPREAD: Temperature Read-back (B8h)

Temperature read-back from the built-in temperature sensing device.
The 1st parameter is dummy data.
The 2nd parameter (TBF and TD6 to TD0): Temperature read busy and temperature value.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	TMPREAD	0	↑	1	1	0	1	1	1	0	0	0	(B8h)
1	Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
1	2nd parameter	1	1	↑	TBF	TD6	TD5	TD4	TD3	TD2	TD1	TD0	-

NOTE: For the relationship between TD [6:0] and temperature, see section "5.11.9 Temperature Compensation".

6.2.34 EPVOL: Electrical Volume set for EEPROM (C0h)

Specify the voltage regulator circuit's electronic volume offset value (which will be stored in EEPROM).
The 1st parameter: Electrical Volume offset value
The 2nd parameter: Dummy byte
The 3rd parameter: Resistance Ratio offset value

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	EPVOL	0	↑	1	1	1	0	0	0	0	0	0	(C0h)
1	1st parameter	1	↑	1	-	-	EOF5	EOF4	EOF3	EOF2	EOF1	EOF0	-
1	2nd parameter	1	↑	1	-	-	-	-	-	-	-	-	Dummy byte
1	2nd parameter	1	↑	1	-	-	-	-	-	ROF2	ROF1	ROF0	-

6.2.35 EPWRIN: EEPROM Write Start (CDh)

Write start the Electronic volume offset (EOF), Resistance ratio (ROF) value and ID2 into the EEPROM.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	EPWRIN	0	↑	1	1	1	0	0	1	1	0	1	(CDh)
1	Parameter	No Parameter											

6.2.36 EPWROUT: EEPROM Write End (CCh)

Write end the Electronic volume offset (EOF), Resistance ratio (ROF) value and ID2 into the EEPROM

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	EPWROUT	0	↑	1	1	1	0	0	1	1	0	0	(CCh)
1	Parameter	No Parameter											

6.2.37 RDEV: Read Electrical Volume Value (7Ch)

This read byte returns 7-bit Electrical Volume Value.
The 1st parameter is dummy data
The 2nd parameter (EV6 to EV0): Internal Electrical Volume Value.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	RDEV	0	↑	1	0	1	1	1	1	1	0	0	(7Ch)
1	Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
1	2nd parameter	1	1	↑	-	EV6	EV5	EV4	EV3	EV2	EV1	EV0	-

6.2.38 RDRR: Read Resistor Ratio Value (7Dh)

This read byte returns 3-bit Resistor Ratio Value.
The 1st parameter is dummy data
The 2nd parameter (RR2 to RR0): Internal Resistor Ratio Value.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	RDRR	0	↑	1	0	1	1	1	1	1	0	1	(7Dh)
1	Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
1	2nd parameter	1	1	↑	-	-	-	-	-	RR2	RR1	RR0	-

6.2.39 RDID1: Read ID1 Value (DAh)

This read byte returns 8-bit LCD module's manufacturer ID
The 1st parameter is dummy data
The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	RDID1	0	↑	1	1	1	0	1	1	0	1	0	(DAh)
1	Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
1	2nd Parameter	1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-

6.2.40 RDID2: Read ID2 Value (DBh)

This read byte returns 8-bit LCD module/driver version ID
The 1st parameter is dummy data
The 2nd parameter (ID26 to ID20): LCD module/driver version ID

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	RDID2	0	↑	1	1	1	0	1	1	0	1	1	(DBh)
1	Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
1	2nd Parameter	1	1	↑	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-

6.2.41 RDID3: Read ID3 Value (DCh)

This read byte returns 8-bit LCD module/driver ID.
The 1st parameter is dummy data
The 2nd parameter (ID37 to ID30): LCD module/driver ID.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	RDID3	0	↑	1	1	1	0	1	1	1	0	0	(DCh)
1	Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
1	2nd Parameter	1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

6.2.42 IDMOFF: Idle Mode Off (38h)

This command is used to recover from Idle mode on.
There will be no abnormal visible effect on the display mode change transition.
In the idle off mode LCD can display maximum 4096 colors and normal frame frequency is applied.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	IDMOFF	0	↑	1	0	0	1	1	1	0	0	0	(38h)
1	Parameter	No Parameter											

6.2.43 IDMON: Idle Mode On (39h)

This command is used to enter into Idle mode on.
There will be no abnormal visible effect on the display mode change transition.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	IDMON	0	↑	1	0	0	1	1	1	0	0	1	(39h)
1	Parameter	No Parameter											

In the idle on mode,
1. Color expression is reduced. The primary and the secondary colors using MSB of each RMG and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command

6.2.44 TEOFF: Tearing Effect Line OFF (34h)

This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	TEOFF	0	↑	1	0	0	1	1	0	1	0	0	(34h)
1	Parameter	No Parameter											

6.2.45 TEON: Tearing Effect Line ON (35h)

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit ML.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	TEON	0	↑	1	0	0	1	1	0	1	0	1	(35h)
1	Parameter	1	↑	1	-	-	-	-	-	-	-	M	-

6.2.46 TEST1: Test Command1 (6-h)

This instruction is a testing instruction code for Leadis. Please do not use it.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	TEST1	0	↑	1	0	1	1	0	-	-	-	-	(6-h)

6.2.47 TEST2: Test Command2 (0-h)

This instruction is a testing instruction code for Leadis. Please do not use it.

ISS	Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
1	TEST2	0	↑	1	0	0	0	0	-	-	-	-	(0-h)

6.3 RESET TABLE (DEFAULT VALUE)

6.3.1 Instruction Code0 (ISS=0)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Booster On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
All Pixel On/Off	Off	Off	Off
Contrast (EV)	3Fh	3Fh	3Fh
Display On/Off	Off	Off	Off
Column: Start Address (XS)	01h	01h	01h
Column: End Address (XE)	82h	82h	82h
Row: Start Address (YS)	01h	01h	01h
Row: End Address (YE)	82h	82h	82h
RGB for 4k and 256 Color Mode (R/G/B)	All 0h	All 0h	**No Change**
Partial: Start Address (PSL)	00h	00h	00h
Partial: End Address (PEL)	80h	80h	80h
Scroll: Top Fixed Area (TFA)	00h	00h	00h
Scroll: Scroll Area (VSA)	84h	84h	84h
Scroll: Bottom Fixed Area (BFA)	00h	00h	00h
Scroll Start Address (SSA)	00h	00h	00h
Tearing: On/Off	Off	Off	Off
Tearing Mode	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	**No Change**
Idle Mode On/Off	Off	Off	Off
Interface Pixel Color Format (P)	3 (12-Bit/Pixel Type A)	3 (12-Bit/Pixel Type A)	**No Change**
Clock Internal/External	Internal	Internal	Internal
Frame Frequency in Normal Color (FA/FB/FC/FD)	03h/07h/07h/07h	03h/07h/07h/07h	03h/07h/07h/07h
Frame Frequency in 8-Color (Idle) (F8A/F8B/F8C/F8D)	03h/07h/07h/07h	03h/07h/07h/07h	03h/07h/07h/07h
Temperature Range (TA/TB/TC)	2Dh/7Fh/7Fh	2Dh/7Fh/7Fh	2Dh/7Fh/7Fh
Temperature Hysteresis (TH)	05h	05h	05h
Display Control: F1/F2 Switching (FS)	07h (field)	07h (field)	07h (field)
Display Control: N-Line Inversion (FINV/NL)	15h	15h	15h
ID1	45h	45h	45h
ID2	80h ~ FFh	80h ~ FFh	80h ~ FFh
ID3	03h	03h	03h

6.3.2 Instruction Code1 (ISS=1)

Item	After Power On	After Hardware Reset
Frame memory	Random	No Change
Sleep In/Out	In	In
Oscillator On/Off	Off	Off
Power Control (PW)	00h (All Off)	00h (All Off)
Partial: Start Line (PSB)	00h	00h
Partial: End Line (PEB)	83h	83h
Display Inversion On/Off	Off	Off
Display On/Off	Off	Off
Column: Start Address (XS)	00h	00h
Column: End Address (XE)	83h	83h
Row: Start Address (YS)	00h	00h
Row: End Address (YE)	83h	83h
RGB for 4k and 256 Color Mode (R/G/B)	All 0h	All 0h
Scroll: Top Scroll Block (SSL)	00h	00h
Scroll: Bottom Scroll Block (SEL)	00h	00h
Scroll: Specified Block (SFL)	00h	00h
Scroll: Scroll Mode (SMD)	3 (Whole Scroll)	3 (Whole Scroll)
Scroll Start Address (SSA)	00h	00h
Data Access Control (MV/MX/MY/RGB)	0/0/0/0	0/0/0/0
Data Access Control (GS)	2 (12-Bit/Pixel Type A)	2 (12-Bit/Pixel Type A)
Read Modify Write In/Out	Out	Out
Volume Control: (EV)	20h	20h
Display Control: F1/F2 Switching (FS)	07h (field)	07h (field)
Display Control: N-Line Inversion (FINV/NL)	15h	15h
Frame Frequency in Normal Color (FA/FB/FC/FD)	03h/07h/07h/07h	03h/07h/07h/07h
Frame Frequency in 8-Color (Idle) (F8A/F8B/F8C/F8D)	03h/07h/07h/07h	03h/07h/07h/07h
Temperature Range (TA/TB/TC)	2Dh/7Fh/7Fh	2Dh/7Fh/7Fh
Temperature Hysteresis (TH)	05h	05h
Idle Mode On/Off	Off	Off
Tearing: On/Off	Off	Off
ID1	45h	45h
ID2	80h ~ FFh	80h ~ FFh
ID3	03h	03h

6.4 INSTRUCTION SETUP FLOW

6.4.1 Initializing with the Built-in Power Supply Circuits

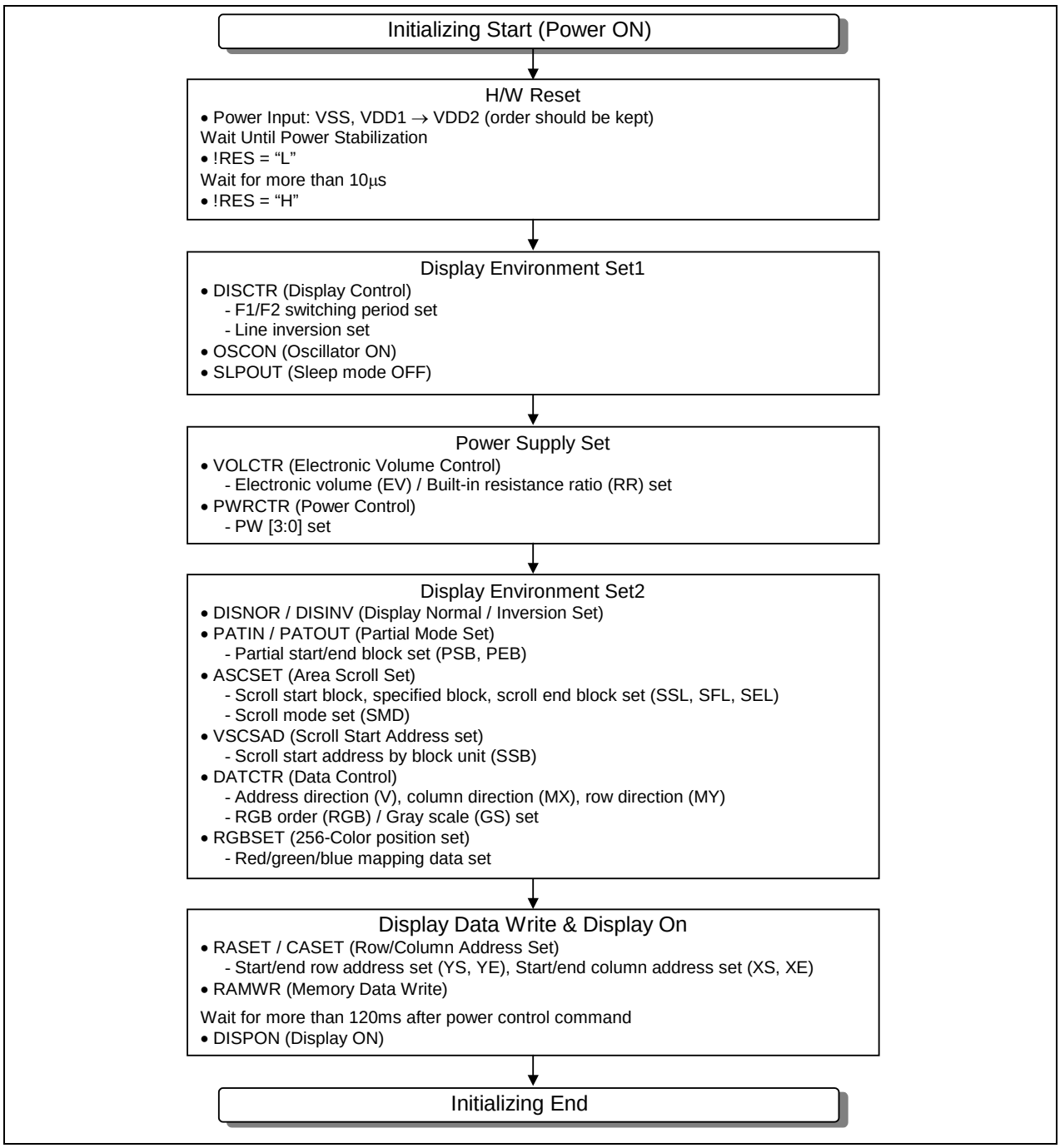


Fig. 6.4.1 Initializing with the built-in power supply circuits (Only for Instruction Code1: ISS="High")

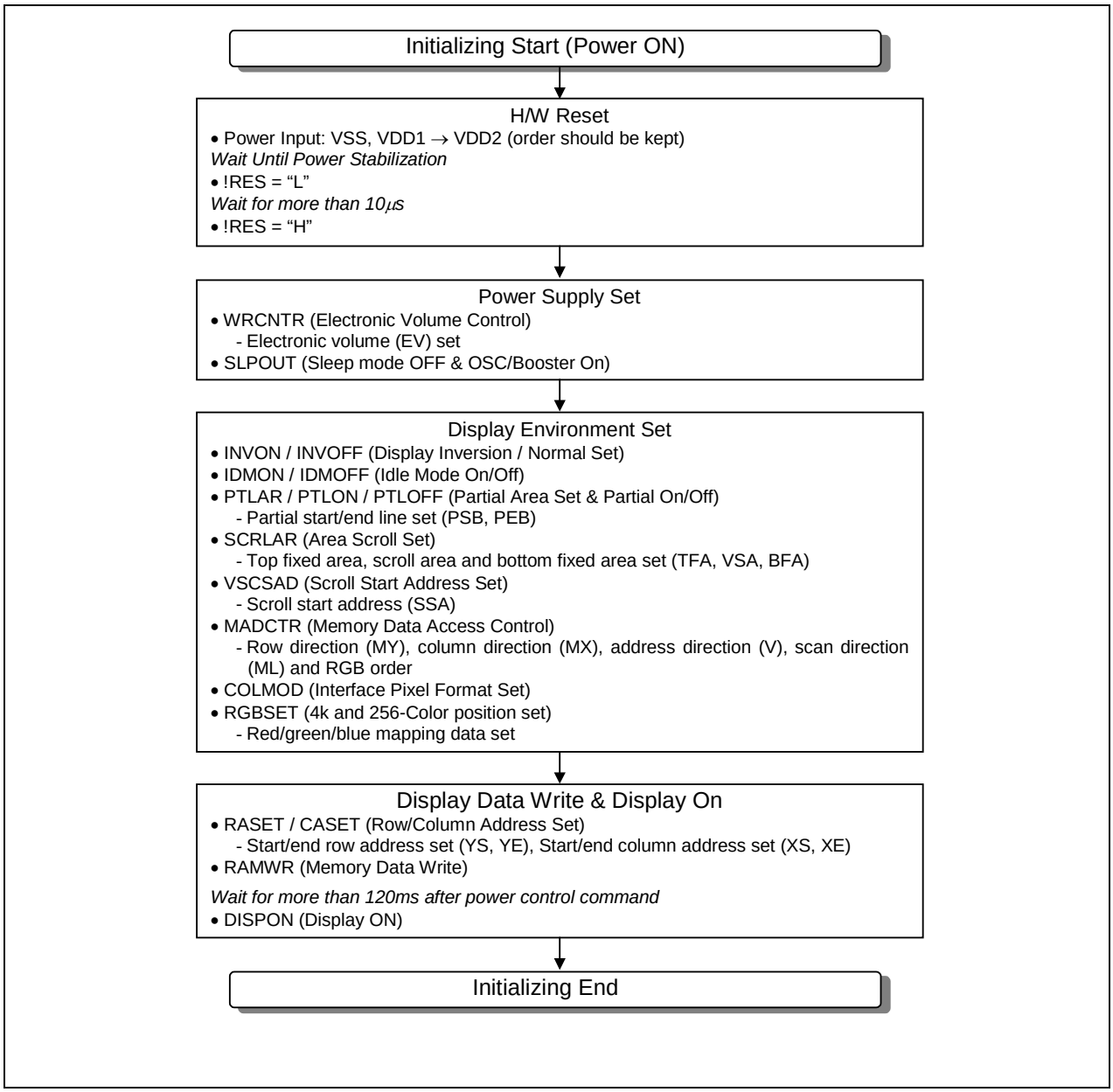


Fig. 6.4.2 Initializing with the built-in power supply circuits (Only for Instruction Code0: ISS="Low")

The initializing sequence does not have any effect on the display. The display is in its normal background color during the initialization.

6.4.2 Power OFF Sequence

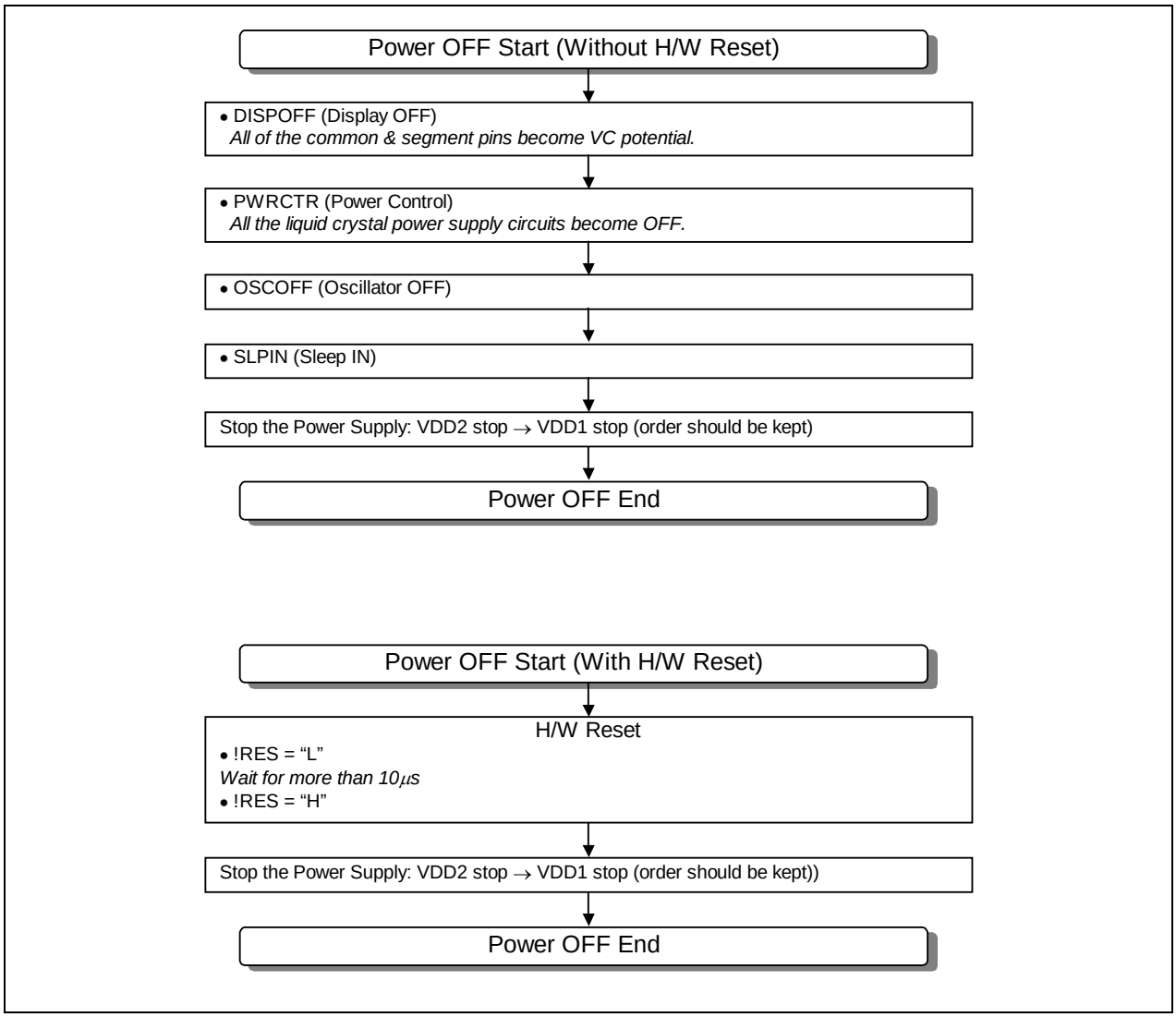


Fig. 6.4.3 Power OFF sequence (Only for Instruction Code1: ISS="High")

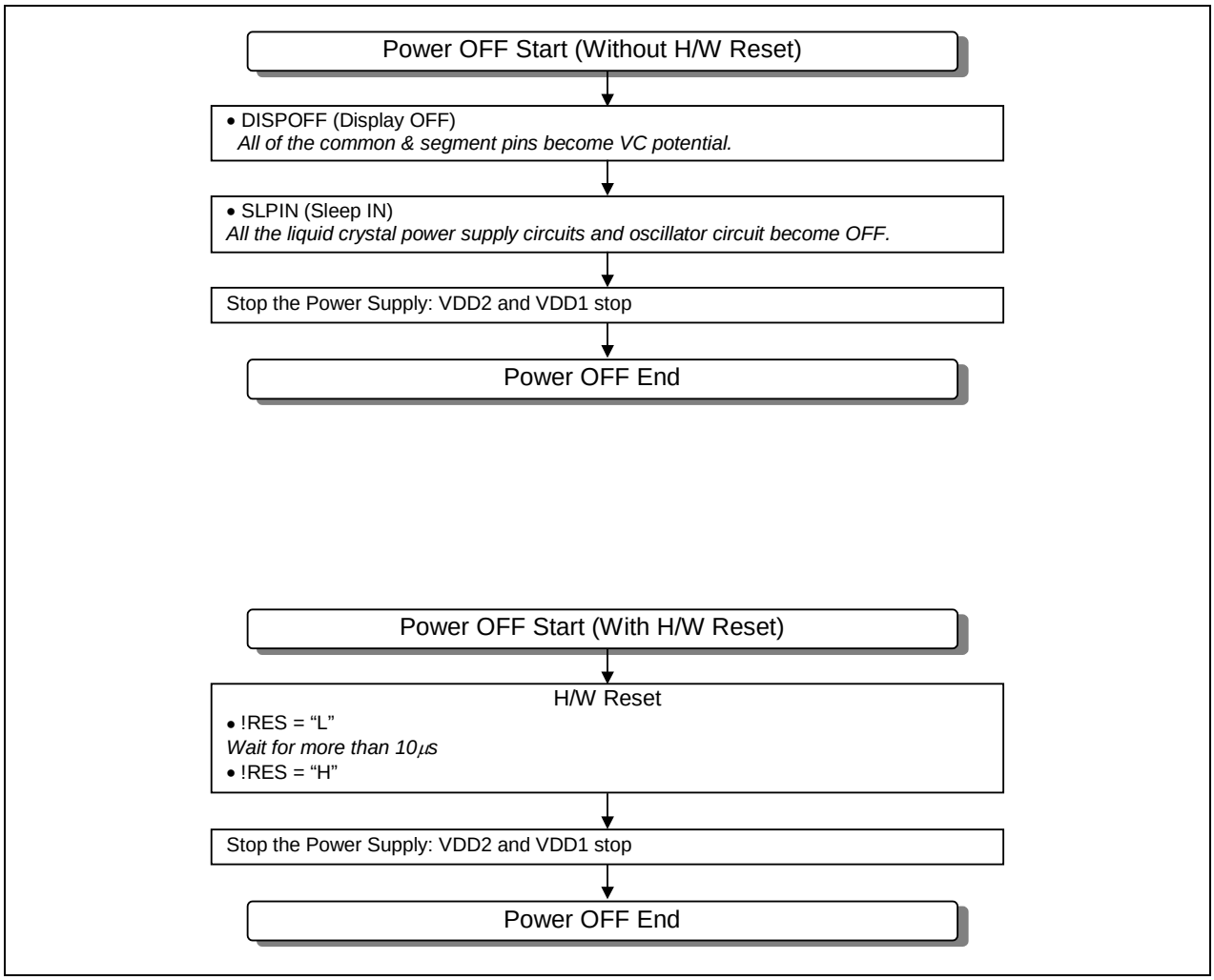


Fig. 6.4.4 Power OFF sequence (Only for Instruction Code0: ISS="Low")

6.4.3 EEPROM Program Sequence

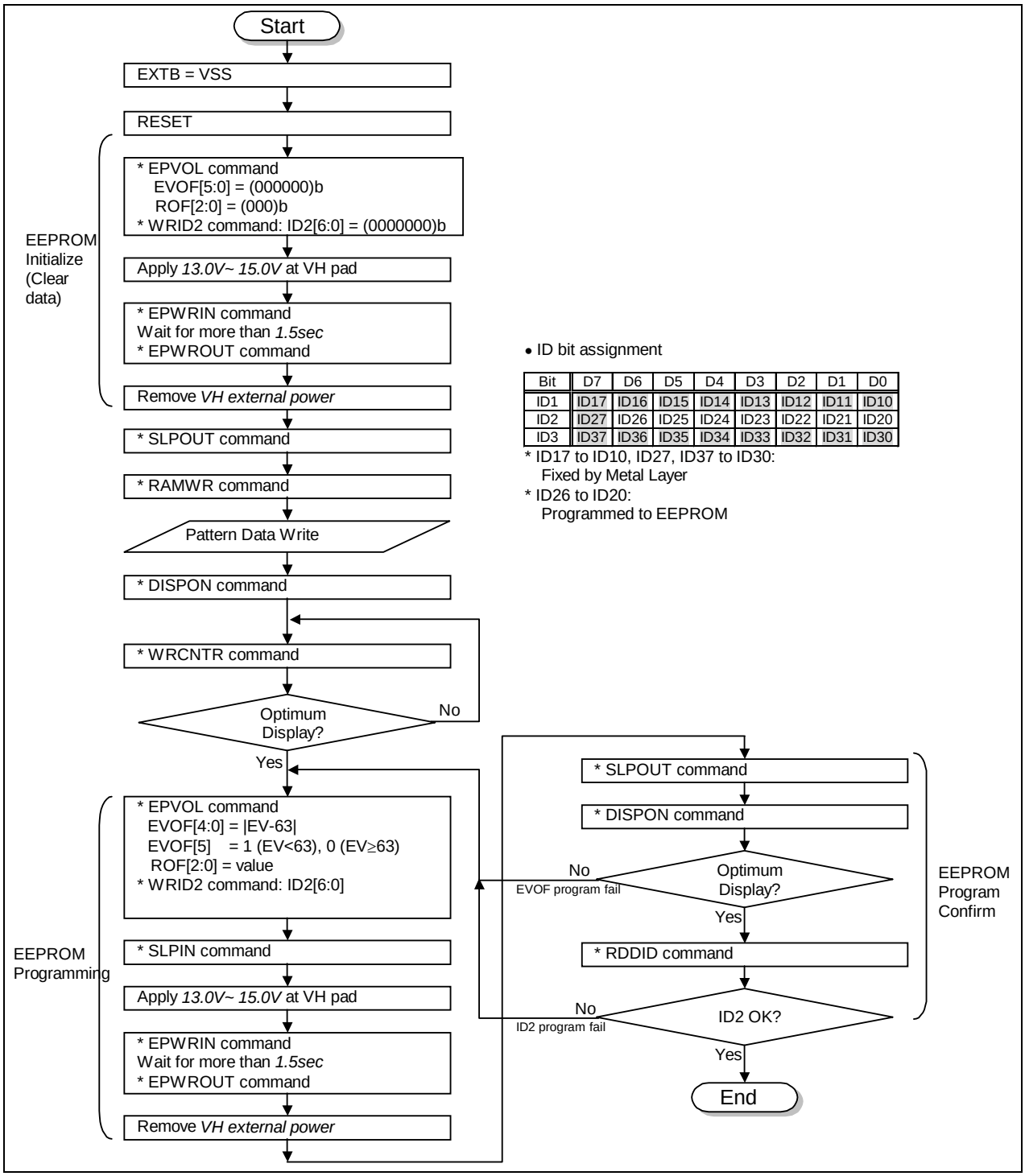


Fig. 6.4.5 EEPROM write/read sequence (For both Instruction Code0 and Code1)

7 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Item	Symbol	Value	Unit
Supply voltage (1)	V_{DD1}, V_{DD2}	- 0.3 ~ + 4.0	V
Supply voltage (2)	V_{LCD} (VH-VL)	- 0.3 ~ + 20.0	V
Supply voltage (3)	V_{MAX} (VH-VOUTL)	- 0.3 ~ + 20.0	V
Input voltage range	V_{IN}	- 0.3 ~ V_{DD} + 0.3	V
Output voltage range	V_O	- 0.3 ~ V_{DD} + 0.3	V
Operating temperature range	T_{OPR}	- 40 ~ + 85	°C
Storage temperature range	T_{STG}	- 55 ~ + 125	°C

NOTE: 1. Voltages are all based on V_{SS} = 0V.

2. Voltage relationship: VH ≥ VXH2 ≥ VXH1 ≥ VC ≥ VXL1 ≥ VXL2 (V_{SS}) ≥ VL ≥ VOUTL must always be satisfied.

7.2 ESD PROTECTION LEVEL

Table 7.2.1 ESD models.

Model	Test Condition	Protection Level	Unit
Human Body Model	C = 100 pF, R = 1.5 kΩ	> 2000	V
Machine Model	C = 200 pF, R = 0.0 Ω	> 200	V

7.3 LATCH-UP PROTECTION LEVEL

The device will not latch up at trigger current levels less than ±100 mA.

7.4 LIGHT SENSITIVITY

The operation of the IC will not be materially altered by incident light.

7.5 MAXIMUM SERIES RESISTANCE

The driver will operate in 'Chip on Glass' applications with series resistances (due to ITO track resistance). Voltages are specified at module I/O assuming maximum values as in ***Table 7.5.1.***

Table 7.5.1 Maximum series resistance on module.

Name	Type	Maximum Series Resistance	Unit
VDD1	Power supply	100	Ω
VDD2	Power supply	50	Ω
VSS	Power supply	50	Ω
VSS1	Power supply	1000	Ω
*1) VH	Capacitor connection	100	Ω
*1) VXH2	Capacitor connection	100	Ω
*1) VXH1	Capacitor connection	100	Ω
*1) VC	Capacitor connection	100	Ω
*1) VXL1	Capacitor connection	100	Ω
*1) VXL2	Capacitor connection	100	Ω
*1) VL	Capacitor connection	100	Ω
OSC, TEST3, TEST4, TEST5, EXTB	Input	1000	Ω
SRGB, SMX, SMY, ROWM	Input	1000	Ω
ISS	Input	1000	Ω
PS0, PS1	Input	1000	Ω
!RES	Input	200	Ω
!CS (!SCE)	Input	200	Ω
D/!C (SCL)	Input	200	Ω
!WR	Input	200	Ω
!RD	Input	200	Ω
TE	Output	1000	Ω
D7 to D0(SDA)	Input / Output	200	Ω
CX1P, CX2P	Capacitor connection	100	Ω
CX1M, CX2M	Capacitor connection	100	Ω
VOUT	Capacitor connection	100	Ω
VOUT2	Capacitor connection	100	Ω
C1P, C2P	Capacitor connection	100	Ω
C1M to C3M	Capacitor connection	100	Ω
VOUTL	Capacitor connection	100	Ω
C5M	Capacitor connection	100	Ω
C5P	Capacitor connection	100	Ω

7.6 DC CHARACTERISTICS

7.6.1 Basic Characteristics

(V_{SS}=0V, V_{DD1}=1.65V to 1.95V, V_{DD2}=2.6V to 2.9V,Ta = -30 to 70°C)

Parameter	Symbol	Conditions	Related Pins	MIN	TYP	MAX	Unit
Logic Operating voltage	V_{DD1}	-	VDD1	1.65	1.8	1.95	V
Analog Operating voltage	V_{DD2}	-	VDD2	2.6	2.75	2.9	
Driving voltage input	V_{LCD}	VH - VL	VH, VL	-	-	18.0	
	V_{MAX}	VH - VOUTL	VH, VOUTL	-	-	18.0	
High level input voltage	V_{IH}		*1)	0.7V_{DD1}	-	V_{DD1}	
Low level input voltage	V_{IL}	-	*1)	V_{SS}	-	0.3V_{DD1}	
High level output voltage	V_{OH}	I_{OH} = -0.5mA	D7 to D0, TE, TEST1	0.8V_{DD1}	-	V_{DD1}	
Low level output voltage	V_{OL}	I_{OL} = +0.5mA		V_{SS}	-	0.2V_{DD1}	
Input leakage current	I_{IL}	V_{IN} = V_{DD1} or V_{SS}	*1)	-1.0	-	+1.0	μA
Driver on resistance (SEG)	R_{ONSEG}	VXH2 = 5.0V	*2) S0 to S395	-	3.5	10	kΩ
Driver on resistance (COM)	R_{ONCOM}	VH = 10.0V	*2) C0 to C131	-	0.4	1.0	
External oscillator frequency	f_{OSC}	DFCL=32	OSC	200.0	211.0	222.0	kHz
Booster1 output voltage range	V_{OUT}	X3, No load	VOUT	7.8	-	8.7	V
	V_{OUT2}	X2, No load	VOUT2	5.2	-	5.8	V
Booster1 output efficiency	V_{OUTEF}	X3, No load	VOUT	95.0	99.0	-	%
	V_{OUT2EF}	X2, No load	VOUT2	95.0	99.0	-	%
Reference voltage	V_{REG}	Ta = 25°C	-	1.55	1.60	1.65	V
Voltage follower output voltage	V_{XH1}	VXH2 = 6.0V	VXH1	4.28	4.50	4.73	V
	V_C		VC	2.85	3.00	3.15	
	V_{XL1}		VXL1	1.43	1.50	1.73	
Booster2 output voltage range	V_{OUTL}	X3, No load	VOUTL	-5.2	-	-5.8	
Booster2 output efficiency	V_{OUTLEF}	X3, No load	VOUTL	95.0	99.0	-	%
Booster3 output efficiency	V_{HEF}	X2, No load	VH	95,0	99.0	-	%

NOTE:

**1) Applies to EXTB, ROWM, OSC, TEST3 to TEST5, ISS, PS0, PS1, !CS, !RES, D/!C(SCL), !WR, !RD, and D7 to D0(SDA) pins*

**2) Resistance value when -0.1[mA] is applied during the ON status of the output pin S0 to S395 and C0 to C131.*

R_{ON} [KΩ] = ΔV[V] / 0.1[mA] (ΔV : Voltage change when –0.1[mA] is applied in the on status.)

7.6.2 Current Consumption

Host I/F	Mode of operation	Frame Frequency	Inversion Mode	Image	Interface Pixel (P[2:0])	Current consumption			
						Typical		Worst case	
						VDD2 (mA)	VDD1 (mA)	VDD2[9] (mA)	VDD1[10] (mA)
Host interface NOT active	- Normal Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode	65Hz		Note 1	X;X;X				
				Note 2	X;X;X				
				Note 3	X;X;X				
				Note 4	X;X;X				
				Note 5	X;X;X				
	- Normal Mode On - Partial Mode Off - Idle Mode On - Sleep Out Mode	65Hz		Note 5	X;X;X				
	- Normal Mode Off - Partial Mode On (32 lines) - Idle Mode Off - Sleep Out Mode	65Hz		Grey Levels	X;X;X				
	- Normal Mode Off - Partial Mode On (32 lines) - Idle Mode On - Sleep Out Mode	65Hz		Note 6	X;X;X				
				Note 7	X;X;X				
	- Sleep In Mode	N/A	N/A	N/A	X;X;X	0.002		0.010	
Host interface active	- Normal Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode		Full screen	4k Colours	0;0;0				
					0;0;1				
				Checker board one by one	0;1;0				
					0;1;1				
				CPU Access @ 10fps	1;0;0				
					1;0;1				
					1;1;0				
					1;1;1				

NOTE:

X Do not care

1. *All pixels black*
2. *Checker board one by one*
3. *Checker board 4 by 4*
4. *Grey-scale from top to bottom*
5. *20% Black, 80%White*
6. *Black & White Checker board 8 by 8.*
7. *Absolute Worst Case Patterns:*
   - *Black & White Horizontal Stripe 1 by 1*
   - *Black & White Checker board 1pixel by 1pixel*
   - *Black & White Checker board 1dot by 1dot*
8. *Absolute worst case VDD2 current is less than 0.8mA in the case of Normal Mode On, Partial Mode Off, Idle Mode Off, Sleep Out mode (CPU access is inactive).*
9. *Absolute worst case VDD1 current is less than 2.0μA in the case of Normal Mode On, Partial Mode Off, Idle Mode Off, Sleep Out mode (Host interface not active).*
10. *Inrush currents are not included in current consumption values*

Typical Case:
T_A = 25ºC
VDD2 = 2.75V
VDD1 = 1.8V

Worst Case:
T_A = -30 to70ºC
VDD2 = 2.6V to 2.9V
VDD1 = 1.65V to 1.95V
Includes Process Variance.

7.7 AC CHARACTERISTICS

7.7.1 Parallel Interface Characteristics (8080-series MPU)

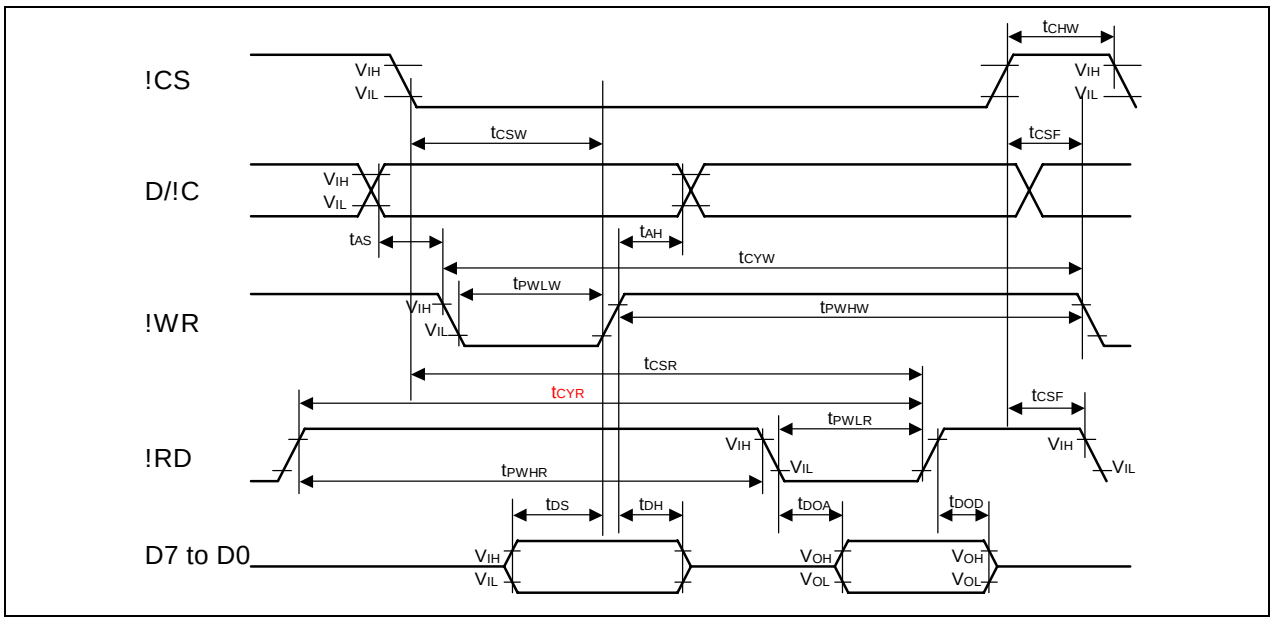


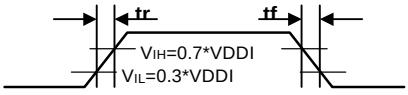
Fig. 7.7.1 Parallel Interface characteristics (8080-series MPU)

(V_{SS}=0V, V_{DD1}=1.65V to 1.95V, V_{DD2}=2.6V to 2.9V,Ta = -30 to 70°C)

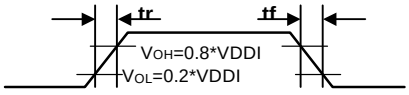
Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CSW}, t_{CSR} t_{CSF} t_{CHW}	Chip select setup time Chip select hold time Chip select high pulse width	-	!CS	40 10 45	- - -	- - -	ns
t_{AS} t_{AH}	Address setup time Address hold time	-	D/!C	10 10	- -	- -	ns
t_{CYW} t_{PWHW} t_{PWLW}	Write cycle time Write High Time Write Low Time	-	!WR	160 90 40	-	-	ns
t_{CYR} t_{PWHR} t_{PWLR}	Read cycle time (Parameter read) Read High (Parameter read) Read Low (Parameter read)	-	!RD	160 90 40	-	-	ns
t_{CYR} t_{PWHR} t_{PWLR}	Read cycle time (Data read) Read High (Data read) Read Low (Data read)	-	!RD	450 90 355	-	-	ns
t_{DS} t_{DH}	Data setup time Data hold time	-	D7 to D0	10 10	- -	- -	ns
t_{DOA} t_{DOD}	Data output access time Data output disable time	CL = 30pF		- 20	- -	40 80	ns

NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Input Signal Slope



Output Signal Slope



7.7.2 Parallel Interface Characteristics (6800-series MPU)

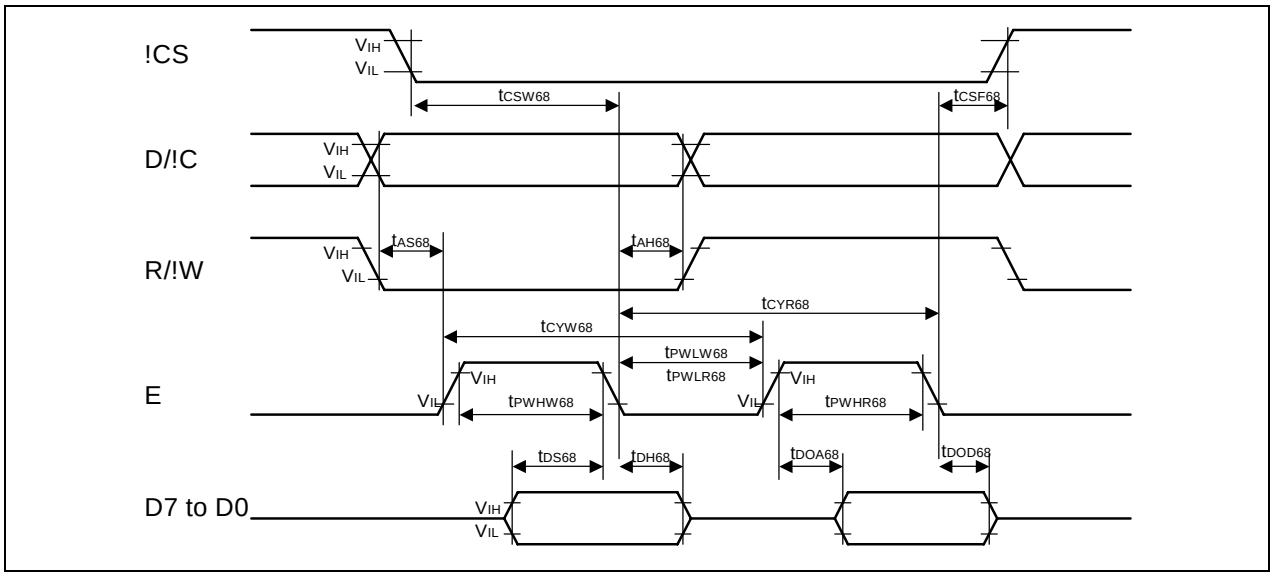


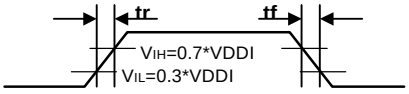
Fig. 7.7.2 Parallel Interface characteristics (6800-series MPU)

(V_{SS}=0V, V_{DD1}=1.65V to 1.95V, V_{DD2}=2.6V to 2.9V,Ta = -30 to 70°C)

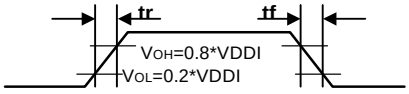
Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CSW68} t_{CSF68}	Chip select setup time Chip select hold time	-	!CS	40 10	- -	- -	ns
t_{AS68} t_{AH68}	Address setup time Address hold time	-	D/!C R/!W	10 10	- -	- -	ns
t_{CYW68} t_{PWHW68} t_{PWLW68}	Write cycle time Write High Time Write Low Time	-	E	160 40 90	-	-	ns
t_{CYR68} t_{PWHR68} t_{PWLR68}	Read cycle time (Parameter read) Read High (Parameter read) Read Low (Parameter read)	-	E	160 40 90	-	-	ns
t_{CYR68} t_{PWHR68} t_{PWLR68}	Read cycle time (Data read) Read High (Data read) Read Low (Data read)	-	E	450 355 90	-	-	ns
t_{DS68} t_{DH68}	Data setup time Data hold time	-	D7 to D0	10 10	- -	- -	ns
t_{DOA68} t_{DOD68}	Data output access time Data output disable time	CL = 30pF		- 20	- -	40 80	ns

NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Input Signal Slope



Output Signal Slope



7.7.3 Serial Interface Characteristics

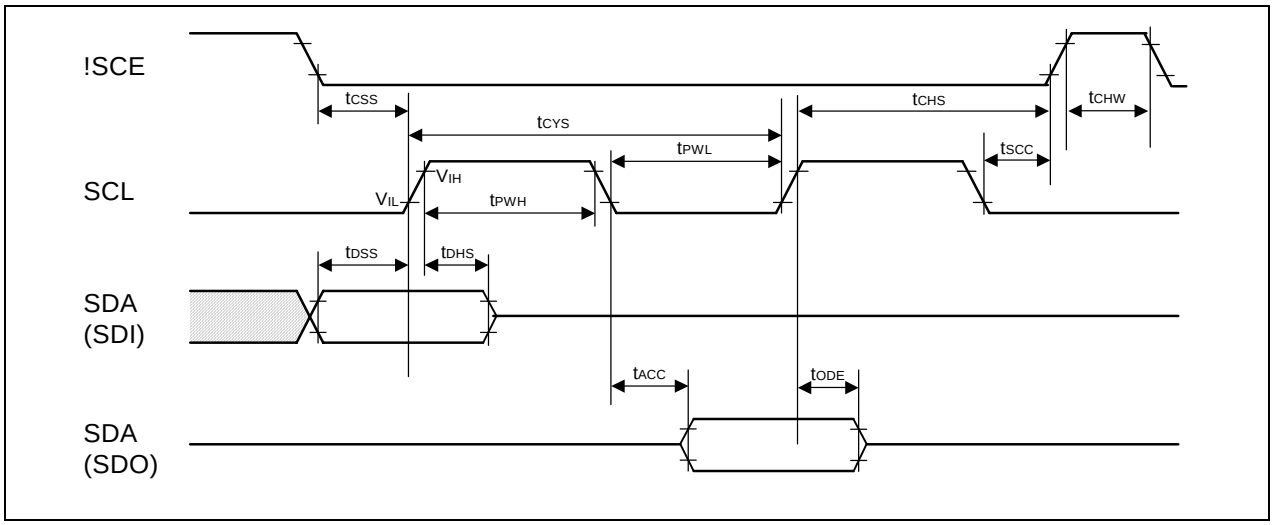


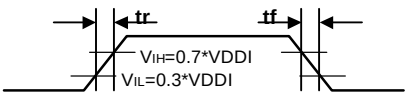
Fig. 7.7.3 Serial interface characteristics

V_{SS}=0V, V_{DD1}=1.65V to 1.95V, V_{DD2}=2.6V to 2.9V,Ta = -30 to 70°C)

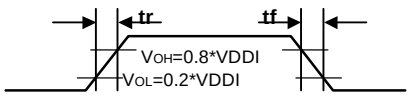
Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CYS} t_{PWH} t_{PWL}	Serial clock cycle Low pulse width High pulse width	-	SCL	150 60 60	- -	- -	ns
t_{DSS} t_{DHS}	Data setup time Data hold time		SDA (SDI)	60 60	- -	- -	ns
t_{CSS} t_{CHS} t_{CHW}	Chip select setup time Chip select hold time Chip select high pulse width	-	!SCE	60 65 45	- - -	- - -	ns
t_{SCC}	SCL to Chip select	-	SCL, !SCE	20	-	-	ns
t_{ACC} t_{ODE}	SDO access time SDO disable time	*1)	SDA (SDO)	10 15	- -	50 50	ns

*NOTE:*1) t_{ACC} condition: Load = 30pF, t_{ODE} condition: Load = 5pF and R = 3kOhm*
The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Input Signal Slope



Output Signal Slope



7.7.4 Reset Input Timing

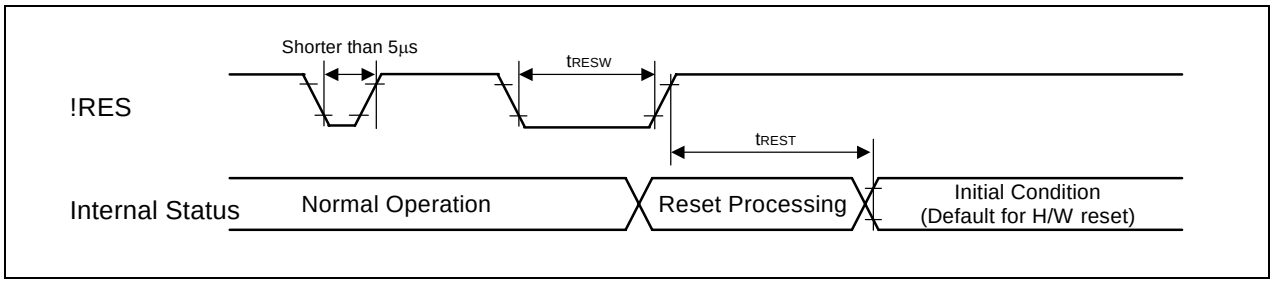


Fig. 7.7.4 Reset input timing

VSS=0V, VDD1=1.65V to 1.95V, VDD2=2.6V to 2.9V,Ta = -30 to 70°C)

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	!RES	10	-	-	-	µs
t_{REST}	*2) Reset complete time	-	-	-	5	-	ms

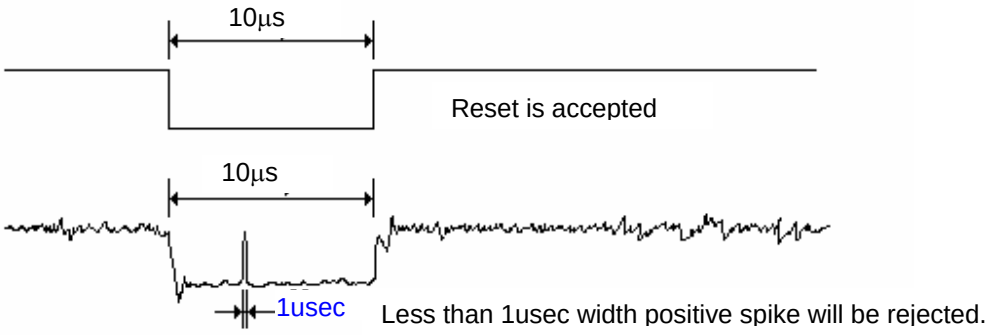
NOTE:

1) Spike due to an electrostatic discharge on !RES line does not cause irregular system reset according to the table below.

!RES Pulse	*Action*
Shorter than 5µs	*Reset Rejected*
Longer than 10µs	*Reset*
Between 5µs and 10µs	*Not Determined*

2) During the resetting period, the display will be blanked and then return to Default condition for H/W reset. (ID2 value in OTP will be latched to internal register during this period)

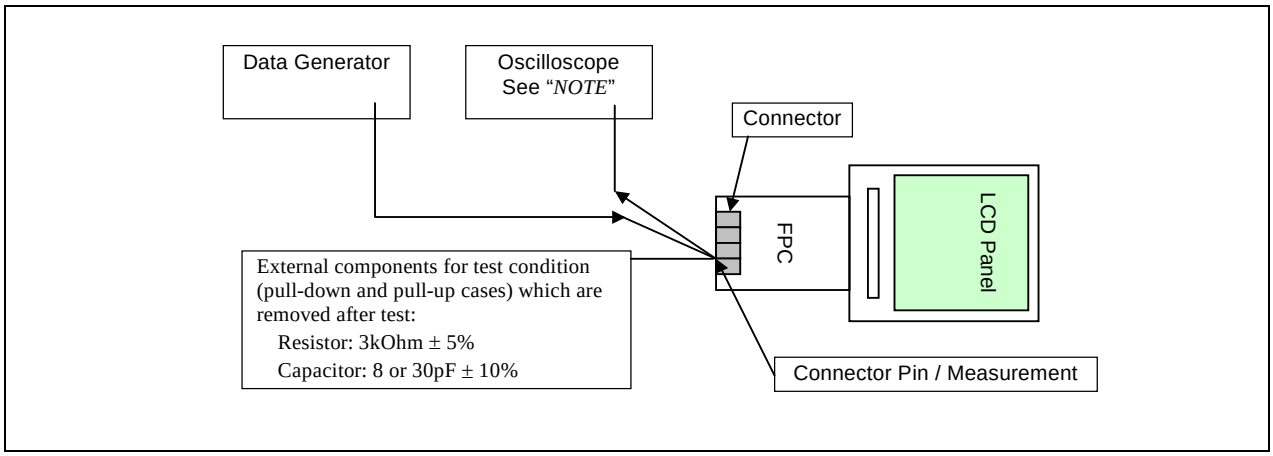
3) Spike Rejection also applies during a valid reset pulse as shown below:



4) It is necessary to wait 10µsec after releasing !RES before sending commands. After reset complete, Sleep Out command can be sent to start internal power circuit.

7.7.5 Measurement Conditions for Parallel and Serial Interfaces

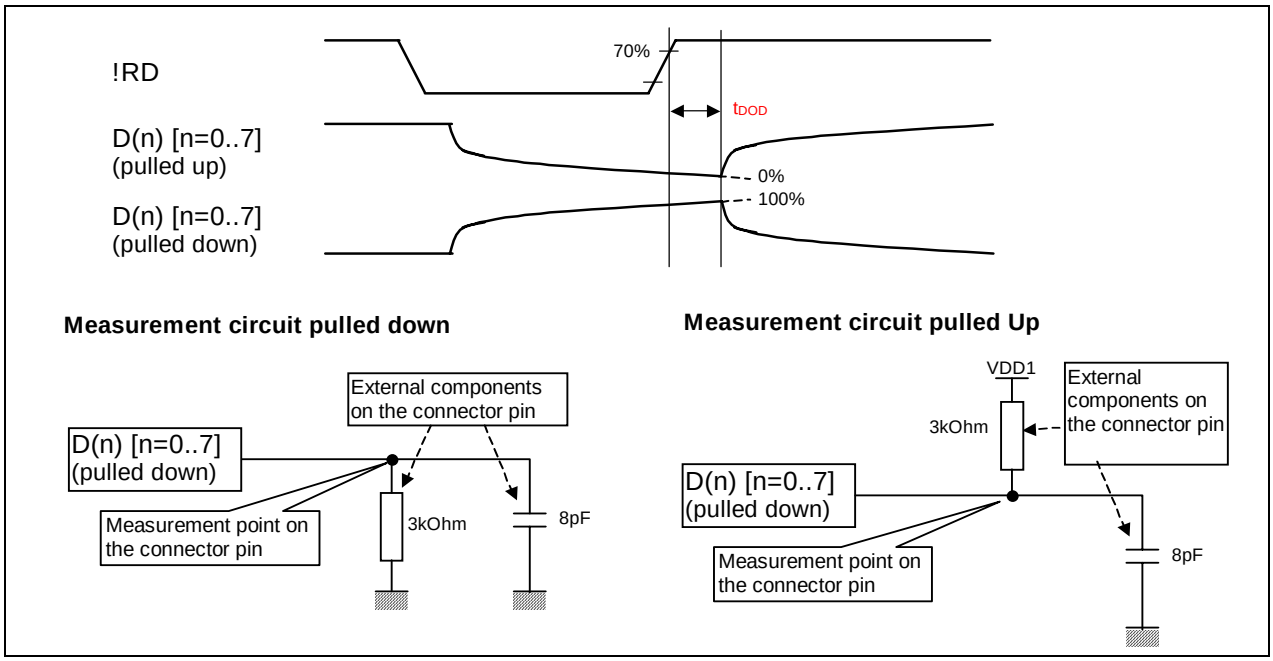
Measurement Condition Set-up for Parallel and Serial Interaces



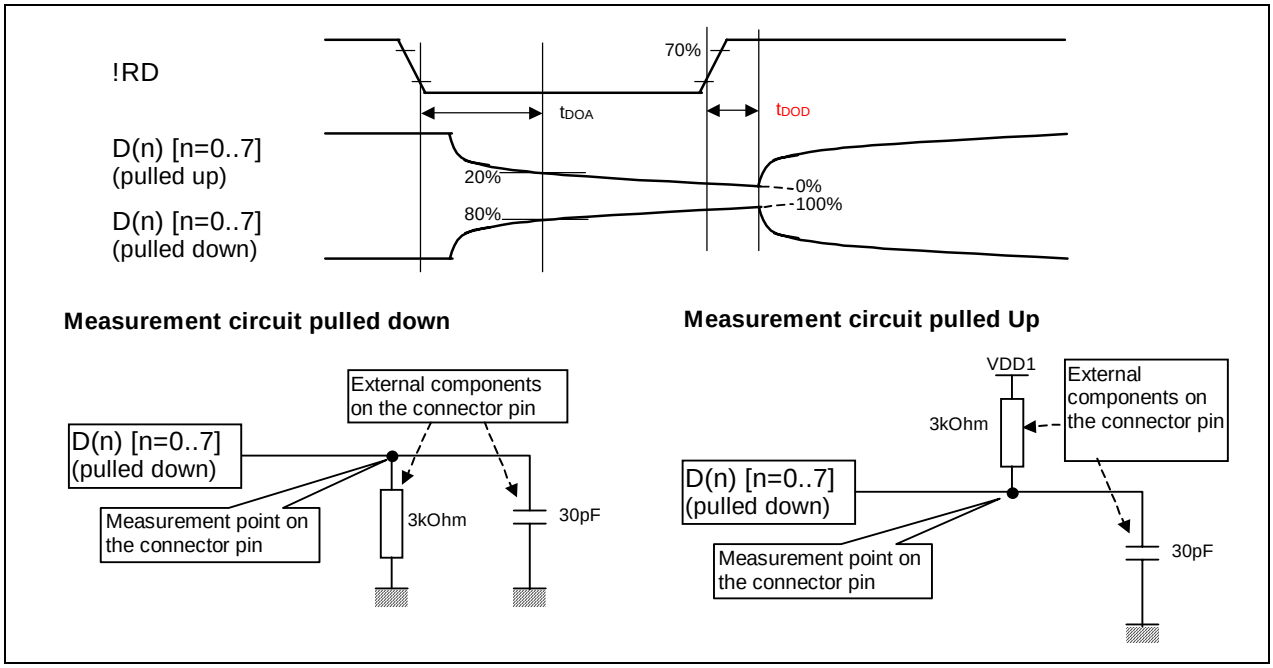
NOTE: Capacitances and resistances of the oscilloscope's probe must be included externals components in these measurements

7.7.5.1 t_{DOA}, t_{DOD} Measurement Condition

Minimum Value Measurement

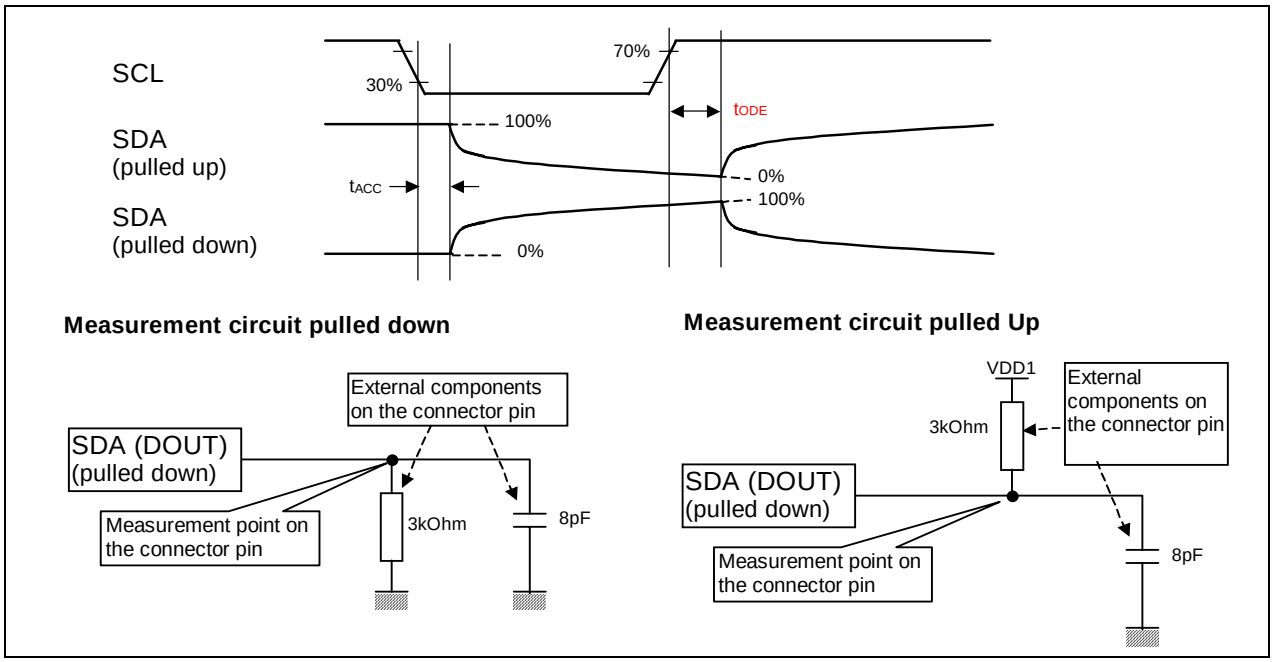


Maximum Value Measurement

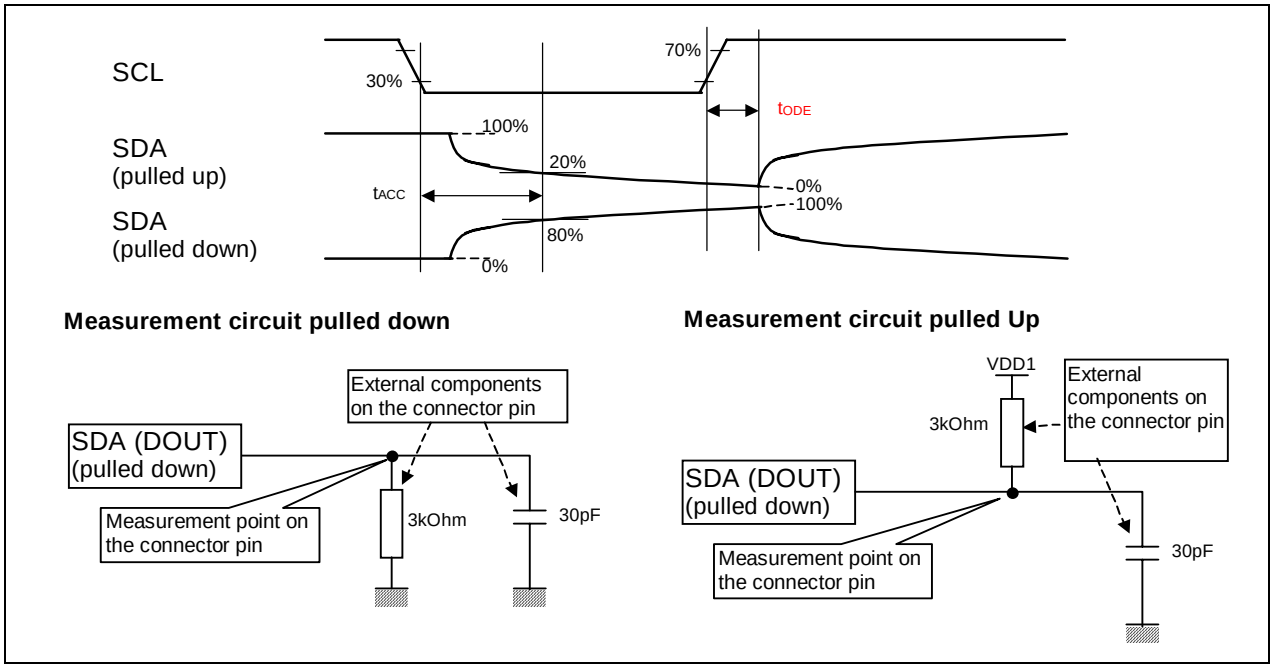


7.7.5.2 t_{ACC}, t_{ODE} Measurement Condition

Minimum Value Measurement



Maximum Value Measurement



8 REFERENCE APPLICATIONS

8.1 MICROPROCESSOR INTERFACE

8.1.1 Interfacing with 8080-series MPU 8-Bit Bus (PS0 = "H", PS1 = "H")

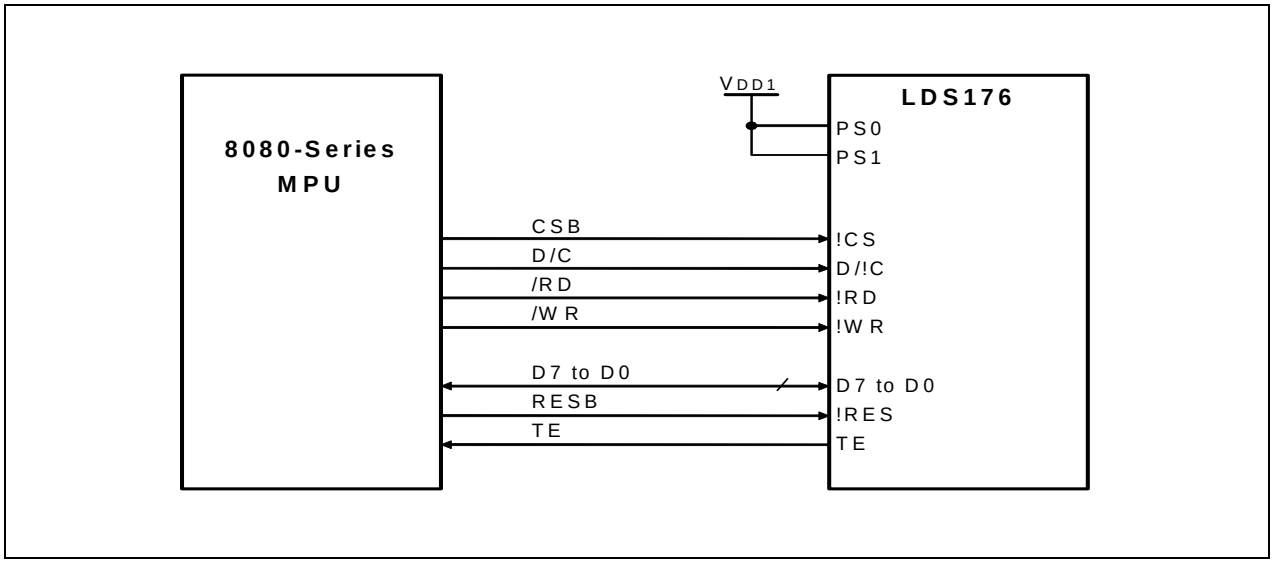


Fig. 8.1.1 Interfacing with 8-bit 8080-series

8.1.2 Interfacing with 6800-series MPU 8-Bit Bus (PS0 = "H", PS1 = "L)

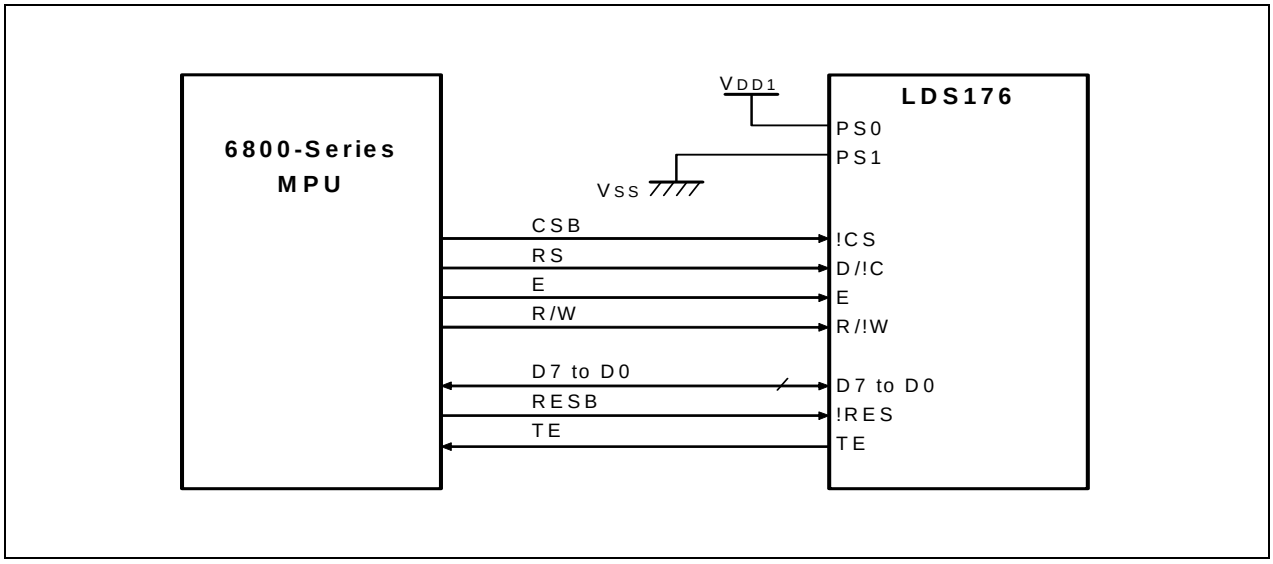


Fig. 8.1.2 Interfacing with 8-bit 6800-series

8.1.3 3-Line Serial mode (PS0 = "L", PS1 = "L" or "H")

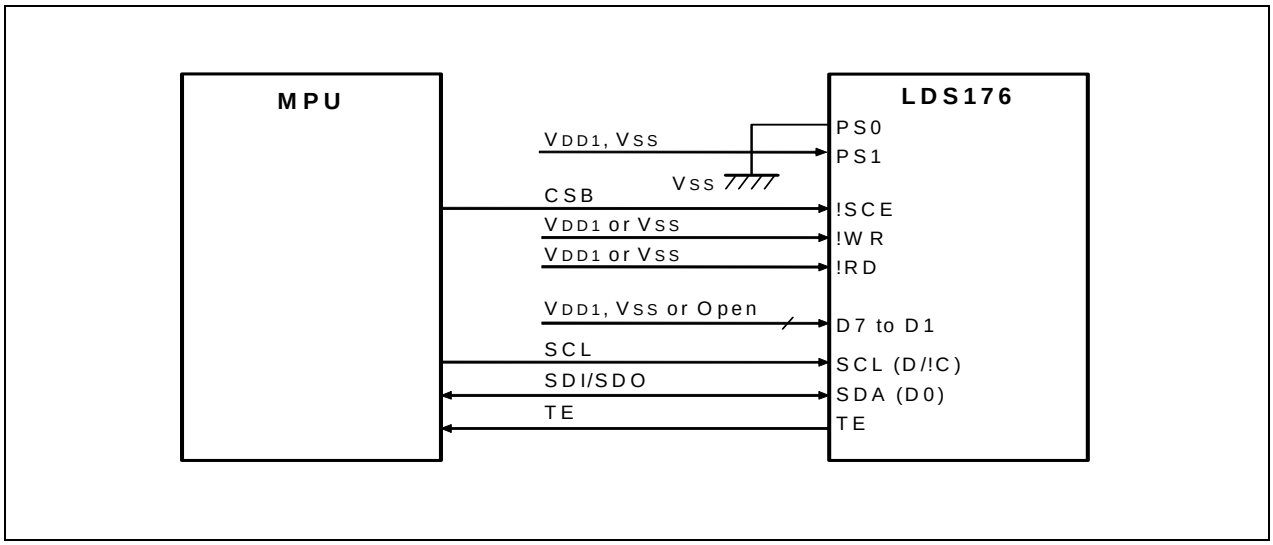
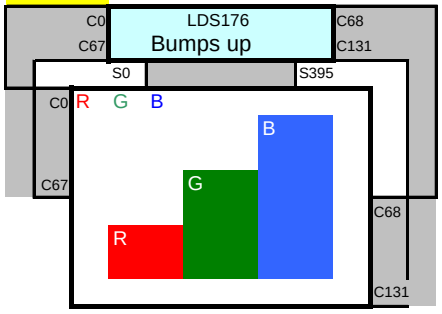


Fig. 8.1.3 3-Line serial interface (PS0 = "L")

8.2 CONNECTIONS WITH LCD PANEL

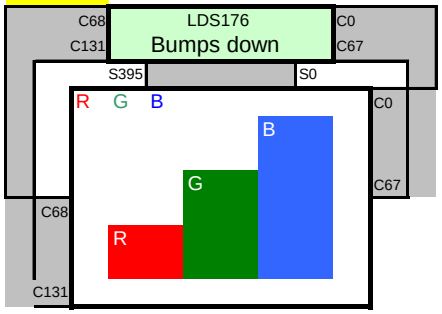
Case 1



MADCTR Command
MX = 0
MY = 0
RGB = 0

S0 = Filter R
S1 = Filter G
S2 = Filter B
…

Case2

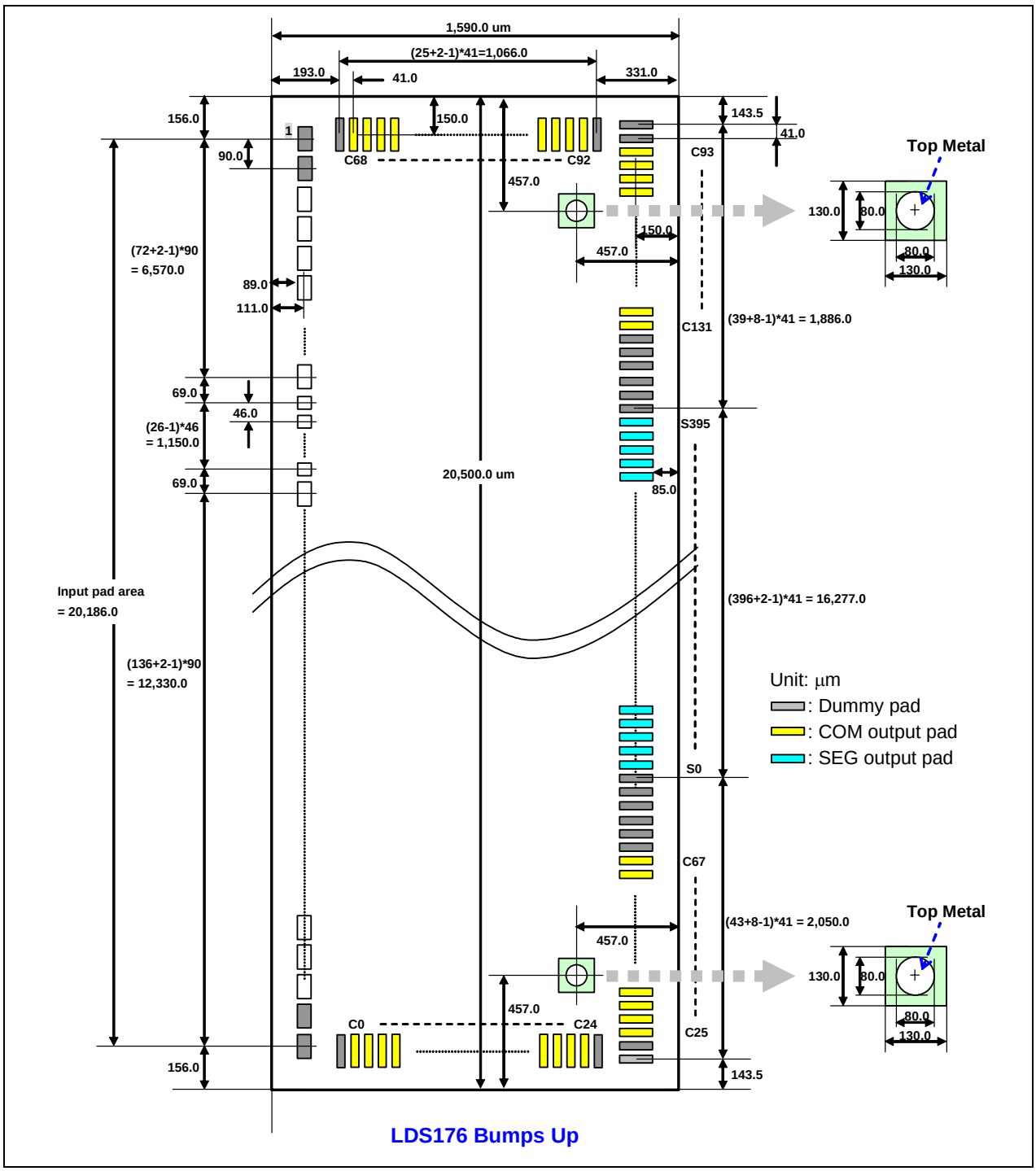


MADCTR Command
MX = 1
MY = 0
RGB = 1

S0 = Filter B
S1 = Filter G
S2 = Filter R
…

9 CHIP INFORMATION

9.1 CHIP OVERVIEW



LDS176 Bumps Up

NOTE:

** Chip Size = 20,500 x 1,590 (Excluding Scribe Lane 200 x 200)*

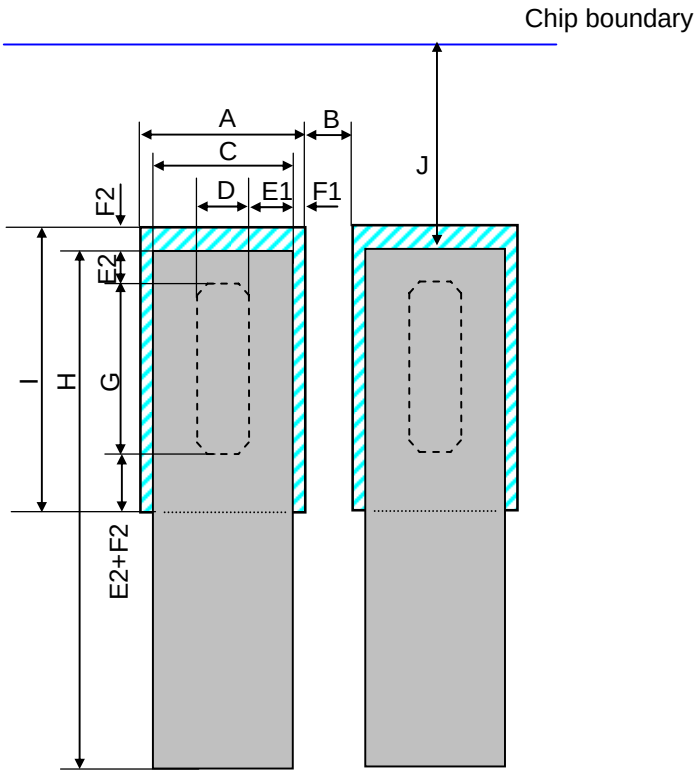
** Chip Thickness = 500 ± 12 μm*

** Bump height = 17 ± 3 μm (chip to chip), less than 2 μm (pad to pad in one chip)*

9.2 BUMP INFORMATION

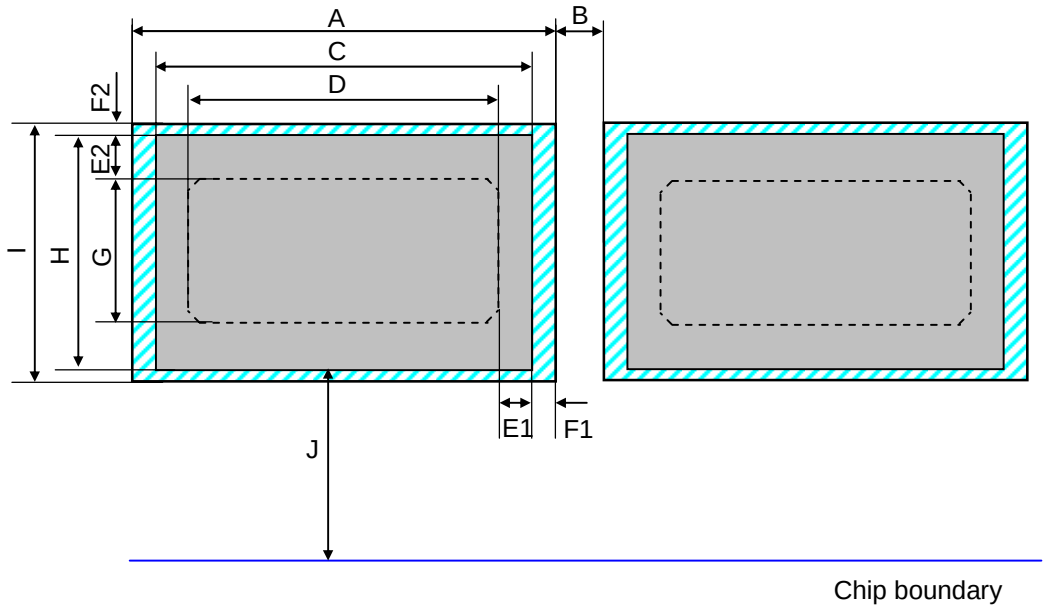
9.2.1 COM/SEG Output Pad Format

Item	Symbol	Size
AL width	A	31μm
AL to AL gap	B	10 μm
Bump width	C	27 μm
Pad open width	D	7 μm
AL height	I	74 μm
Bump height	H	130 μm
Pad open height	G	50 μm
Pad open to Bump gap	E1	10 μm
	E2	7 μm
Bump to AL gap	F1	2 μm
	F2	5 μm
Pad pitch	A+B	41 μm
Bump area	C*H	3,510 μm^2
Chip boundary to Bump edge	J	85 μm



9.2.2 Input Pad Format

Item	Symbol	Size	Size (TESTF)
AL width	A	80 μm	36 μm
AL to AL gap	B	10 μm	10 μm
Bump width	C	70 μm	26 μm
Pad open width	D	56 μm	12 μm
AL height	I	62 μm	62 μm
Bump height	H	58 μm	58 μm
Pad open height	G	38 μm	38 μm
Pad open to Bump gap	E1	7 μm	7 μm
	E2	10 μm	10 μm
Bump to AL gap	F1	5 μm	5 μm
	F2	2 μm	2 μm
Pad pitch	A+B	90 μm	46 μm
Bump area	C*H	4,060 μm^2	1,508 μm^2
Chip boundary to Bump edge	J	86 μm	86 μm



9.3 PAD COORDINATES

Table 9.3.1 Pad Center Coordinates

No	Name	X	Y	No	Name	X	Y
1	DUMMY	-10094.0	-680.0	51	VOUT	-5594.0	-680.0
2	DUMMY	-10004.0	-680.0	52	VOUT	-5504.0	-680.0
3	VH	-9914.0	-680.0	53	EXTB	-5414.0	-680.0
4	VH	-9824.0	-680.0	54	EXTB	-5324.0	-680.0
5	VH	-9734.0	-680.0	55	!RES	-5234.0	-680.0
6	VH	-9644.0	-680.0	56	!RES	-5144.0	-680.0
7	VXH2	-9554.0	-680.0	57	!CS	-5054.0	-680.0
8	VXH2	-9464.0	-680.0	58	!CS	-4964.0	-680.0
9	VXH2	-9374.0	-680.0	59	VSS	-4874.0	-680.0
10	VXH2	-9284.0	-680.0	60	VSS	-4784.0	-680.0
11	VXH1	-9194.0	-680.0	61	VSS	-4694.0	-680.0
12	VXH1	-9104.0	-680.0	62	VSS	-4604.0	-680.0
13	VXH1	-9014.0	-680.0	63	VSS	-4514.0	-680.0
14	VXH1	-8924.0	-680.0	64	VSS	-4424.0	-680.0
15	VC	-8834.0	-680.0	65	VSS	-4334.0	-680.0
16	VC	-8744.0	-680.0	66	VSS	-4244.0	-680.0
17	VC	-8654.0	-680.0	67	VSS	-4154.0	-680.0
18	VC	-8564.0	-680.0	68	VSS	-4064.0	-680.0
19	VXL1	-8474.0	-680.0	69	VSS	-3974.0	-680.0
20	VXL1	-8384.0	-680.0	70	VSS	-3884.0	-680.0
21	VXL1	-8294.0	-680.0	71	VSS1	-3794.0	-680.0
22	VXL1	-8204.0	-680.0	72	VSS1	-3704.0	-680.0
23	VXL2	-8114.0	-680.0	73	TE	-3614.0	-680.0
24	VXL2	-8024.0	-680.0	74	TE	-3524.0	-680.0
25	VXL2	-7934.0	-680.0	75	TESTF1	-3455.0	-680.0
26	VXL2	-7844.0	-680.0	76	TESTF2	-3409.0	-680.0
27	DUMMY	-7754.0	-680.0	77	TESTF3	-3363.0	-680.0
28	VLL	-7664.0	-680.0	78	TESTF4	-3317.0	-680.0
29	VLL	-7574.0	-680.0	79	TESTF5	-3271.0	-680.0
30	VLL	-7484.0	-680.0	80	TESTF6	-3225.0	-680.0
31	VLL	-7394.0	-680.0	81	TESTF7	-3179.0	-680.0
32	DUMMY	-7304.0	-680.0	82	TESTF8	-3133.0	-680.0
33	CX2M	-7214.0	-680.0	83	TESTF9	-3087.0	-680.0
34	CX2M	-7124.0	-680.0	84	TESTF10	-3041.0	-680.0
35	CX2M	-7034.0	-680.0	85	TESTF11	-2995.0	-680.0
36	CX1M	-6944.0	-680.0	86	TESTF12	-2949.0	-680.0
37	CX1M	-6854.0	-680.0	87	TESTF13	-2903.0	-680.0
38	CX1M	-6764.0	-680.0	88	TESTF14	-2857.0	-680.0
39	CX1P	-6674.0	-680.0	89	TESTF15	-2811.0	-680.0
40	CX1P	-6584.0	-680.0	90	TESTF16	-2765.0	-680.0
41	CX1P	-6494.0	-680.0	91	TESTF17	-2719.0	-680.0
42	VOUT2	-6404.0	-680.0	92	TESTF18	-2673.0	-680.0
43	VOUT2	-6314.0	-680.0	93	TESTF19	-2627.0	-680.0
44	VOUT2	-6224.0	-680.0	94	TESTF20	-2581.0	-680.0
45	VOUT2	-6134.0	-680.0	95	TESTF21	-2535.0	-680.0
46	CX2P	-6044.0	-680.0	96	TESTF22	-2489.0	-680.0
47	CX2P	-5954.0	-680.0	97	TESTF23	-2443.0	-680.0
48	CX2P	-5864.0	-680.0	98	TESTF24	-2397.0	-680.0
49	VOUT	-5774.0	-680.0	99	TESTF25	-2351.0	-680.0
50	VOUT	-5684.0	-680.0	100	TESTF26	-2305.0	-680.0

Table 9.3.2 Pad Center Coordinates (Continued)

No	Name	X	Y	No	Name	X	Y
101	OSC	-2236.0	-680.0	151	VCAP2	2264.0	-680.0
102	OSC	-2146.0	-680.0	152	VCAP2	2354.0	-680.0
103	TEST7	-2056.0	-680.0	153	VCAP2	2444.0	-680.0
104	TEST7	-1966.0	-680.0	154	VCAP1	2534.0	-680.0
105	TEST7	-1876.0	-680.0	155	VCAP1	2624.0	-680.0
106	TEST7	-1786.0	-680.0	156	VCAP1	2714.0	-680.0
107	TEST7	-1696.0	-680.0	157	VCAP1	2804.0	-680.0
108	TEST7	-1606.0	-680.0	158	VCAP1	2894.0	-680.0
109	ISS	-1516.0	-680.0	159	VCAP1	2984.0	-680.0
110	ISS	-1426.0	-680.0	160	VCAP1	3074.0	-680.0
111	PS0	-1336.0	-680.0	161	VCAP1	3164.0	-680.0
112	PS0	-1246.0	-680.0	162	VCAP1	3254.0	-680.0
113	PS1	-1156.0	-680.0	163	VCAP1	3344.0	-680.0
114	PS1	-1066.0	-680.0	164	VCAP1	3434.0	-680.0
115	TEST6	-976.0	-680.0	165	C3M	3524.0	-680.0
116	TEST6	-886.0	-680.0	166	C3M	3614.0	-680.0
117	TEST8	-796.0	-680.0	167	C3M	3704.0	-680.0
118	TEST8	-706.0	-680.0	168	DB0	3794.0	-680.0
119	TEST8	-616.0	-680.0	169	DB0	3884.0	-680.0
120	TEST8	-526.0	-680.0	170	D/!C	3974.0	-680.0
121	TEST8	-436.0	-680.0	171	D/!C	4064.0	-680.0
122	TEST8	-346.0	-680.0	172	VDD1	4154.0	-680.0
123	!RD	-256.0	-680.0	173	VDD1	4244.0	-680.0
124	!RD	-166.0	-680.0	174	VDD1	4334.0	-680.0
125	!WR	-76.0	-680.0	175	VDD1	4424.0	-680.0
126	!WR	14.0	-680.0	176	VDD2	4514.0	-680.0
127	TEST1	104.0	-680.0	177	VDD2	4604.0	-680.0
128	TEST1	194.0	-680.0	178	VDD2	4694.0	-680.0
129	DB7	284.0	-680.0	179	VDD2	4784.0	-680.0
130	DB7	374.0	-680.0	180	VDD2	4874.0	-680.0
131	DB6	464.0	-680.0	181	VDD2	4964.0	-680.0
132	DB6	554.0	-680.0	182	VDD2	5054.0	-680.0
133	DB5	644.0	-680.0	183	VDD2	5144.0	-680.0
134	DB5	734.0	-680.0	184	VDD2	5234.0	-680.0
135	DB4	824.0	-680.0	185	VDD2	5324.0	-680.0
136	DB4	914.0	-680.0	186	C2P	5414.0	-680.0
137	DB3	1004.0	-680.0	187	C2P	5504.0	-680.0
138	DB3	1094.0	-680.0	188	C2P	5594.0	-680.0
139	DB2	1184.0	-680.0	189	C1P	5684.0	-680.0
140	DB2	1274.0	-680.0	190	C1P	5774.0	-680.0
141	DB1	1364.0	-680.0	191	C1P	5864.0	-680.0
142	DB1	1454.0	-680.0	192	C2M	5954.0	-680.0
143	VCAP2	1544.0	-680.0	193	C2M	6044.0	-680.0
144	VCAP2	1634.0	-680.0	194	C2M	6134.0	-680.0
145	VCAP2	1724.0	-680.0	195	C1M	6224.0	-680.0
146	VCAP2	1814.0	-680.0	196	C1M	6314.0	-680.0
147	VCAP2	1904.0	-680.0	197	C1M	6404.0	-680.0
148	VCAP2	1994.0	-680.0	198	C5M	6494.0	-680.0
149	VCAP2	2084.0	-680.0	199	C5M	6584.0	-680.0
150	VCAP2	2174.0	-680.0	200	C5M	6674.0	-680.0

Table 9.3.3 Pad Center Coordinates (Continued)

No	Name	X	Y	No	Name	X	Y
201	VOUTL	6764.0	-680.0	251	COM11	10100.0	-110.0
202	VOUTL	6854.0	-680.0	252	COM12	10100.0	-69.0
203	VOUTL	6944.0	-680.0	253	COM13	10100.0	-28.0
204	VLR	7034.0	-680.0	254	COM14	10100.0	13.0
205	VLR	7124.0	-680.0	255	COM15	10100.0	54.0
206	VLR	7214.0	-680.0	256	COM16	10100.0	95.0
207	VLR	7304.0	-680.0	257	COM17	10100.0	136.0
208	DUMMY	7394.0	-680.0	258	COM18	10100.0	177.0
209	VXL2	7484.0	-680.0	259	COM19	10100.0	218.0
210	VXL2	7574.0	-680.0	260	COM20	10100.0	259.0
211	VXL2	7664.0	-680.0	261	COM21	10100.0	300.0
212	VXL2	7754.0	-680.0	262	COM22	10100.0	341.0
213	VXL1	7844.0	-680.0	263	COM23	10100.0	382.0
214	VXL1	7934.0	-680.0	264	COM24	10100.0	423.0
215	VXL1	8024.0	-680.0	265	DUMMY	10100.0	464.0
216	VXL1	8114.0	-680.0	266	DUMMY	10106.5	645.0
217	VC	8204.0	-680.0	267	DUMMY	10065.5	645.0
218	VC	8294.0	-680.0	268	COM25	10024.5	645.0
219	VC	8384.0	-680.0	269	COM26	9983.5	645.0
220	VC	8474.0	-680.0	270	COM27	9942.5	645.0
221	VXH1	8564.0	-680.0	271	COM28	9901.5	645.0
222	VXH1	8654.0	-680.0	272	COM29	9860.5	645.0
223	VXH1	8744.0	-680.0	273	COM30	9819.5	645.0
224	VXH1	8834.0	-680.0	274	COM31	9778.5	645.0
225	VXH2	8924.0	-680.0	275	COM32	9737.5	645.0
226	VXH2	9014.0	-680.0	276	COM33	9696.5	645.0
227	VXH2	9104.0	-680.0	277	COM34	9655.5	645.0
228	VXH2	9194.0	-680.0	278	COM35	9614.5	645.0
229	VH	9284.0	-680.0	279	COM36	9573.5	645.0
230	VH	9374.0	-680.0	280	COM37	9532.5	645.0
231	VH	9464.0	-680.0	281	COM38	9491.5	645.0
232	VH	9554.0	-680.0	282	COM39	9450.5	645.0
233	C5P	9644.0	-680.0	283	COM40	9409.5	645.0
234	C5P	9734.0	-680.0	284	COM41	9368.5	645.0
235	C5P	9824.0	-680.0	285	COM42	9327.5	645.0
236	C5P	9914.0	-680.0	286	COM43	9286.5	645.0
237	DUMMY	10004.0	-680.0	287	COM44	9245.5	645.0
238	DUMMY	10094.0	-680.0	288	COM45	9204.5	645.0
239	DUMMY	10100.0	-602.0	289	COM46	9163.5	645.0
240	COM0	10100.0	-561.0	290	COM47	9122.5	645.0
241	COM1	10100.0	-520.0	291	COM48	9081.5	645.0
242	COM2	10100.0	-479.0	292	COM49	9040.5	645.0
243	COM3	10100.0	-438.0	293	COM50	8999.5	645.0
244	COM4	10100.0	-397.0	294	COM51	8958.5	645.0
245	COM5	10100.0	-356.0	295	COM52	8917.5	645.0
246	COM6	10100.0	-315.0	296	COM53	8876.5	645.0
247	COM7	10100.0	-274.0	297	COM54	8835.5	645.0
248	COM8	10100.0	-233.0	298	COM55	8794.5	645.0
249	COM9	10100.0	-192.0	299	COM56	8753.5	645.0
250	COM10	10100.0	-151.0	300	COM57	8712.5	645.0

Table 9.3.4 Pad Center Coordinates (Continued)

No	Name	X	Y	No	Name	X	Y
301	COM58	8671.5	645.0	351	SEG34	6621.5	645.0
302	COM59	8630.5	645.0	352	SEG35	6580.5	645.0
303	COM60	8589.5	645.0	353	SEG36	6539.5	645.0
304	COM61	8548.5	645.0	354	SEG37	6498.5	645.0
305	COM62	8507.5	645.0	355	SEG38	6457.5	645.0
306	COM63	8466.5	645.0	356	SEG39	6416.5	645.0
307	COM64	8425.5	645.0	357	SEG40	6375.5	645.0
308	COM65	8384.5	645.0	358	SEG41	6334.5	645.0
309	COM66	8343.5	645.0	359	SEG42	6293.5	645.0
310	COM67	8302.5	645.0	360	SEG43	6252.5	645.0
311	DUMMY	8261.5	645.0	361	SEG44	6211.5	645.0
312	DUMMY	8220.5	645.0	362	SEG45	6170.5	645.0
313	DUMMY	8179.5	645.0	363	SEG46	6129.5	645.0
314	DUMMY	8138.5	645.0	364	SEG47	6088.5	645.0
315	DUMMY	8097.5	645.0	365	SEG48	6047.5	645.0
316	DUMMY	8056.5	645.0	366	SEG49	6006.5	645.0
317	SEG0	8015.5	645.0	367	SEG50	5965.5	645.0
318	SEG1	7974.5	645.0	368	SEG51	5924.5	645.0
319	SEG2	7933.5	645.0	369	SEG52	5883.5	645.0
320	SEG3	7892.5	645.0	370	SEG53	5842.5	645.0
321	SEG4	7851.5	645.0	371	SEG54	5801.5	645.0
322	SEG5	7810.5	645.0	372	SEG55	5760.5	645.0
323	SEG6	7769.5	645.0	373	SEG56	5719.5	645.0
324	SEG7	7728.5	645.0	374	SEG57	5678.5	645.0
325	SEG8	7687.5	645.0	375	SEG58	5637.5	645.0
326	SEG9	7646.5	645.0	376	SEG59	5596.5	645.0
327	SEG10	7605.5	645.0	377	SEG60	5555.5	645.0
328	SEG11	7564.5	645.0	378	SEG61	5514.5	645.0
329	SEG12	7523.5	645.0	379	SEG62	5473.5	645.0
330	SEG13	7482.5	645.0	380	SEG63	5432.5	645.0
331	SEG14	7441.5	645.0	381	SEG64	5391.5	645.0
332	SEG15	7400.5	645.0	382	SEG65	5350.5	645.0
333	SEG16	7359.5	645.0	383	SEG66	5309.5	645.0
334	SEG17	7318.5	645.0	384	SEG67	5268.5	645.0
335	SEG18	7277.5	645.0	385	SEG68	5227.5	645.0
336	SEG19	7236.5	645.0	386	SEG69	5186.5	645.0
337	SEG20	7195.5	645.0	387	SEG70	5145.5	645.0
338	SEG21	7154.5	645.0	388	SEG71	5104.5	645.0
339	SEG22	7113.5	645.0	389	SEG72	5063.5	645.0
340	SEG23	7072.5	645.0	390	SEG73	5022.5	645.0
341	SEG24	7031.5	645.0	391	SEG74	4981.5	645.0
342	SEG25	6990.5	645.0	392	SEG75	4940.5	645.0
343	SEG26	6949.5	645.0	393	SEG76	4899.5	645.0
344	SEG27	6908.5	645.0	394	SEG77	4858.5	645.0
345	SEG28	6867.5	645.0	395	SEG78	4817.5	645.0
346	SEG29	6826.5	645.0	396	SEG79	4776.5	645.0
347	SEG30	6785.5	645.0	397	SEG80	4735.5	645.0
348	SEG31	6744.5	645.0	398	SEG81	4694.5	645.0
349	SEG32	6703.5	645.0	399	SEG82	4653.5	645.0
350	SEG33	6662.5	645.0	400	SEG83	4612.5	645.0

Table 9.3.5 Pad Center Coordinates (Continued)

No	Name	X	Y	No	Name	X	Y
401	SEG84	4571.5	645.0	451	SEG134	2521.5	645.0
402	SEG85	4530.5	645.0	452	SEG135	2480.5	645.0
403	SEG86	4489.5	645.0	453	SEG136	2439.5	645.0
404	SEG87	4448.5	645.0	454	SEG137	2398.5	645.0
405	SEG88	4407.5	645.0	455	SEG138	2357.5	645.0
406	SEG89	4366.5	645.0	456	SEG139	2316.5	645.0
407	SEG90	4325.5	645.0	457	SEG140	2275.5	645.0
408	SEG91	4284.5	645.0	458	SEG141	2234.5	645.0
409	SEG92	4243.5	645.0	459	SEG142	2193.5	645.0
410	SEG93	4202.5	645.0	460	SEG143	2152.5	645.0
411	SEG94	4161.5	645.0	461	SEG144	2111.5	645.0
412	SEG95	4120.5	645.0	462	SEG145	2070.5	645.0
413	SEG96	4079.5	645.0	463	SEG146	2029.5	645.0
414	SEG97	4038.5	645.0	464	SEG147	1988.5	645.0
415	SEG98	3997.5	645.0	465	SEG148	1947.5	645.0
416	SEG99	3956.5	645.0	466	SEG149	1906.5	645.0
417	SEG100	3915.5	645.0	467	SEG150	1865.5	645.0
418	SEG101	3874.5	645.0	468	SEG151	1824.5	645.0
419	SEG102	3833.5	645.0	469	SEG152	1783.5	645.0
420	SEG103	3792.5	645.0	470	SEG153	1742.5	645.0
421	SEG104	3751.5	645.0	471	SEG154	1701.5	645.0
422	SEG105	3710.5	645.0	472	SEG155	1660.5	645.0
423	SEG106	3669.5	645.0	473	SEG156	1619.5	645.0
424	SEG107	3628.5	645.0	474	SEG157	1578.5	645.0
425	SEG108	3587.5	645.0	475	SEG158	1537.5	645.0
426	SEG109	3546.5	645.0	476	SEG159	1496.5	645.0
427	SEG110	3505.5	645.0	477	SEG160	1455.5	645.0
428	SEG111	3464.5	645.0	478	SEG161	1414.5	645.0
429	SEG112	3423.5	645.0	479	SEG162	1373.5	645.0
430	SEG113	3382.5	645.0	480	SEG163	1332.5	645.0
431	SEG114	3341.5	645.0	481	SEG164	1291.5	645.0
432	SEG115	3300.5	645.0	482	SEG165	1250.5	645.0
433	SEG116	3259.5	645.0	483	SEG166	1209.5	645.0
434	SEG117	3218.5	645.0	484	SEG167	1168.5	645.0
435	SEG118	3177.5	645.0	485	SEG168	1127.5	645.0
436	SEG119	3136.5	645.0	486	SEG169	1086.5	645.0
437	SEG120	3095.5	645.0	487	SEG170	1045.5	645.0
438	SEG121	3054.5	645.0	488	SEG171	1004.5	645.0
439	SEG122	3013.5	645.0	489	SEG172	963.5	645.0
440	SEG123	2972.5	645.0	490	SEG173	922.5	645.0
441	SEG124	2931.5	645.0	491	SEG174	881.5	645.0
442	SEG125	2890.5	645.0	492	SEG175	840.5	645.0
443	SEG126	2849.5	645.0	493	SEG176	799.5	645.0
444	SEG127	2808.5	645.0	494	SEG177	758.5	645.0
445	SEG128	2767.5	645.0	495	SEG178	717.5	645.0
446	SEG129	2726.5	645.0	496	SEG179	676.5	645.0
447	SEG130	2685.5	645.0	497	SEG180	635.5	645.0
448	SEG131	2644.5	645.0	498	SEG181	594.5	645.0
449	SEG132	2603.5	645.0	499	SEG182	553.5	645.0
450	SEG133	2562.5	645.0	500	SEG183	512.5	645.0

Table 9.3.6 Pad Center Coordinates (Continued)

No	Name	X	Y	No	Name	X	Y
501	SEG184	471.5	645.0	551	SEG234	-1578.5	645.0
502	SEG185	430.5	645.0	552	SEG235	-1619.5	645.0
503	SEG186	389.5	645.0	553	SEG236	-1660.5	645.0
504	SEG187	348.5	645.0	554	SEG237	-1701.5	645.0
505	SEG188	307.5	645.0	555	SEG238	-1742.5	645.0
506	SEG189	266.5	645.0	556	SEG239	-1783.5	645.0
507	SEG190	225.5	645.0	557	SEG240	-1824.5	645.0
508	SEG191	184.5	645.0	558	SEG241	-1865.5	645.0
509	SEG192	143.5	645.0	559	SEG242	-1906.5	645.0
510	SEG193	102.5	645.0	560	SEG243	-1947.5	645.0
511	SEG194	61.5	645.0	561	SEG244	-1988.5	645.0
512	SEG195	20.5	645.0	562	SEG245	-2029.5	645.0
513	SEG196	-20.5	645.0	563	SEG246	-2070.5	645.0
514	SEG197	-61.5	645.0	564	SEG247	-2111.5	645.0
515	SEG198	-102.5	645.0	565	SEG248	-2152.5	645.0
516	SEG199	-143.5	645.0	566	SEG249	-2193.5	645.0
517	SEG200	-184.5	645.0	567	SEG250	-2234.5	645.0
518	SEG201	-225.5	645.0	568	SEG251	-2275.5	645.0
519	SEG202	-266.5	645.0	569	SEG252	-2316.5	645.0
520	SEG203	-307.5	645.0	570	SEG253	-2357.5	645.0
521	SEG204	-348.5	645.0	571	SEG254	-2398.5	645.0
522	SEG205	-389.5	645.0	572	SEG255	-2439.5	645.0
523	SEG206	-430.5	645.0	573	SEG256	-2480.5	645.0
524	SEG207	-471.5	645.0	574	SEG257	-2521.5	645.0
525	SEG208	-512.5	645.0	575	SEG258	-2562.5	645.0
526	SEG209	-553.5	645.0	576	SEG259	-2603.5	645.0
527	SEG210	-594.5	645.0	577	SEG260	-2644.5	645.0
528	SEG211	-635.5	645.0	578	SEG261	-2685.5	645.0
529	SEG212	-676.5	645.0	579	SEG262	-2726.5	645.0
530	SEG213	-717.5	645.0	580	SEG263	-2767.5	645.0
531	SEG214	-758.5	645.0	581	SEG264	-2808.5	645.0
532	SEG215	-799.5	645.0	582	SEG265	-2849.5	645.0
533	SEG216	-840.5	645.0	583	SEG266	-2890.5	645.0
534	SEG217	-881.5	645.0	584	SEG267	-2931.5	645.0
535	SEG218	-922.5	645.0	585	SEG268	-2972.5	645.0
536	SEG219	-963.5	645.0	586	SEG269	-3013.5	645.0
537	SEG220	-1004.5	645.0	587	SEG270	-3054.5	645.0
538	SEG221	-1045.5	645.0	588	SEG271	-3095.5	645.0
539	SEG222	-1086.5	645.0	589	SEG272	-3136.5	645.0
540	SEG223	-1127.5	645.0	590	SEG273	-3177.5	645.0
541	SEG224	-1168.5	645.0	591	SEG274	-3218.5	645.0
542	SEG225	-1209.5	645.0	592	SEG275	-3259.5	645.0
543	SEG226	-1250.5	645.0	593	SEG276	-3300.5	645.0
544	SEG227	-1291.5	645.0	594	SEG277	-3341.5	645.0
545	SEG228	-1332.5	645.0	595	SEG278	-3382.5	645.0
546	SEG229	-1373.5	645.0	596	SEG279	-3423.5	645.0
547	SEG230	-1414.5	645.0	597	SEG280	-3464.5	645.0
548	SEG231	-1455.5	645.0	598	SEG281	-3505.5	645.0
549	SEG232	-1496.5	645.0	599	SEG282	-3546.5	645.0
550	SEG233	-1537.5	645.0	600	SEG283	-3587.5	645.0

Table 9.3.7 Pad Center Coordinates (Continued)

No	Name	X	Y	No	Name	X	Y
601	SEG284	-3628.5	645.0	651	SEG334	-5678.5	645.0
602	SEG285	-3669.5	645.0	652	SEG335	-5719.5	645.0
603	SEG286	-3710.5	645.0	653	SEG336	-5760.5	645.0
604	SEG287	-3751.5	645.0	654	SEG337	-5801.5	645.0
605	SEG288	-3792.5	645.0	655	SEG338	-5842.5	645.0
606	SEG289	-3833.5	645.0	656	SEG339	-5883.5	645.0
607	SEG290	-3874.5	645.0	657	SEG340	-5924.5	645.0
608	SEG291	-3915.5	645.0	658	SEG341	-5965.5	645.0
609	SEG292	-3956.5	645.0	659	SEG342	-6006.5	645.0
610	SEG293	-3997.5	645.0	660	SEG343	-6047.5	645.0
611	SEG294	-4038.5	645.0	661	SEG344	-6088.5	645.0
612	SEG295	-4079.5	645.0	662	SEG345	-6129.5	645.0
613	SEG296	-4120.5	645.0	663	SEG346	-6170.5	645.0
614	SEG297	-4161.5	645.0	664	SEG347	-6211.5	645.0
615	SEG298	-4202.5	645.0	665	SEG348	-6252.5	645.0
616	SEG299	-4243.5	645.0	666	SEG349	-6293.5	645.0
617	SEG300	-4284.5	645.0	667	SEG350	-6334.5	645.0
618	SEG301	-4325.5	645.0	668	SEG351	-6375.5	645.0
619	SEG302	-4366.5	645.0	669	SEG352	-6416.5	645.0
620	SEG303	-4407.5	645.0	670	SEG353	-6457.5	645.0
621	SEG304	-4448.5	645.0	671	SEG354	-6498.5	645.0
622	SEG305	-4489.5	645.0	672	SEG355	-6539.5	645.0
623	SEG306	-4530.5	645.0	673	SEG356	-6580.5	645.0
624	SEG307	-4571.5	645.0	674	SEG357	-6621.5	645.0
625	SEG308	-4612.5	645.0	675	SEG358	-6662.5	645.0
626	SEG309	-4653.5	645.0	676	SEG359	-6703.5	645.0
627	SEG310	-4694.5	645.0	677	SEG360	-6744.5	645.0
628	SEG311	-4735.5	645.0	678	SEG361	-6785.5	645.0
629	SEG312	-4776.5	645.0	679	SEG362	-6826.5	645.0
630	SEG313	-4817.5	645.0	680	SEG363	-6867.5	645.0
631	SEG314	-4858.5	645.0	681	SEG364	-6908.5	645.0
632	SEG315	-4899.5	645.0	682	SEG365	-6949.5	645.0
633	SEG316	-4940.5	645.0	683	SEG366	-6990.5	645.0
634	SEG317	-4981.5	645.0	684	SEG367	-7031.5	645.0
635	SEG318	-5022.5	645.0	685	SEG368	-7072.5	645.0
636	SEG319	-5063.5	645.0	686	SEG369	-7113.5	645.0
637	SEG320	-5104.5	645.0	687	SEG370	-7154.5	645.0
638	SEG321	-5145.5	645.0	688	SEG371	-7195.5	645.0
639	SEG322	-5186.5	645.0	689	SEG372	-7236.5	645.0
640	SEG323	-5227.5	645.0	690	SEG373	-7277.5	645.0
641	SEG324	-5268.5	645.0	691	SEG374	-7318.5	645.0
642	SEG325	-5309.5	645.0	692	SEG375	-7359.5	645.0
643	SEG326	-5350.5	645.0	693	SEG376	-7400.5	645.0
644	SEG327	-5391.5	645.0	694	SEG377	-7441.5	645.0
645	SEG328	-5432.5	645.0	695	SEG378	-7482.5	645.0
646	SEG329	-5473.5	645.0	696	SEG379	-7523.5	645.0
647	SEG330	-5514.5	645.0	697	SEG380	-7564.5	645.0
648	SEG331	-5555.5	645.0	698	SEG381	-7605.5	645.0
649	SEG332	-5596.5	645.0	699	SEG382	-7646.5	645.0
650	SEG333	-5637.5	645.0	700	SEG383	-7687.5	645.0

Table 9.3.8 Pad Center Coordinates (Continued)

No	Name	X	Y	No	Name	X	Y
701	SEG384	-7728.5	645.0	751	COM99	-9778.5	645.0
702	SEG385	-7769.5	645.0	752	COM98	-9819.5	645.0
703	SEG386	-7810.5	645.0	753	COM97	-9860.5	645.0
704	SEG387	-7851.5	645.0	754	COM96	-9901.5	645.0
705	SEG388	-7892.5	645.0	755	COM95	-9942.5	645.0
706	SEG389	-7933.5	645.0	756	COM94	-9983.5	645.0
707	SEG390	-7974.5	645.0	757	COM93	-10024.5	645.0
708	SEG391	-8015.5	645.0	758	DUMMY	-10065.5	645.0
709	SEG392	-8056.5	645.0	759	DUMMY	-10106.5	645.0
710	SEG393	-8097.5	645.0	760	DUMMY	-10100.0	464.0
711	SEG394	-8138.5	645.0	761	COM92	-10100.0	423.0
712	SEG395	-8179.5	645.0	762	COM91	-10100.0	382.0
713	DUMMY	-8220.5	645.0	763	COM90	-10100.0	341.0
714	DUMMY	-8261.5	645.0	764	COM89	-10100.0	300.0
715	DUMMY	-8302.5	645.0	765	COM88	-10100.0	259.0
716	DUMMY	-8343.5	645.0	766	COM87	-10100.0	218.0
717	DUMMY	-8384.5	645.0	767	COM86	-10100.0	177.0
718	DUMMY	-8425.5	645.0	768	COM85	-10100.0	136.0
719	COM131	-8466.5	645.0	769	COM84	-10100.0	95.0
720	COM130	-8507.5	645.0	770	COM83	-10100.0	54.0
721	COM129	-8548.5	645.0	771	COM82	-10100.0	13.0
722	COM128	-8589.5	645.0	772	COM81	-10100.0	-28.0
723	COM127	-8630.5	645.0	773	COM80	-10100.0	-69.0
724	COM126	-8671.5	645.0	774	COM79	-10100.0	-110.0
725	COM125	-8712.5	645.0	775	COM78	-10100.0	-151.0
726	COM124	-8753.5	645.0	776	COM77	-10100.0	-192.0
727	COM123	-8794.5	645.0	777	COM76	-10100.0	-233.0
728	COM122	-8835.5	645.0	778	COM75	-10100.0	-274.0
729	COM121	-8876.5	645.0	779	COM74	-10100.0	-315.0
730	COM120	-8917.5	645.0	780	COM73	-10100.0	-356.0
731	COM119	-8958.5	645.0	781	COM72	-10100.0	-397.0
732	COM118	-8999.5	645.0	782	COM71	-10100.0	-438.0
733	COM117	-9040.5	645.0	783	COM70	-10100.0	-479.0
734	COM116	-9081.5	645.0	784	COM69	-10100.0	-520.0
735	COM115	-9122.5	645.0	785	COM68	-10100.0	-561.0
736	COM114	-9163.5	645.0	786	DUMMY	-10100.0	-602.0
737	COM113	-9204.5	645.0				
738	COM112	-9245.5	645.0				
739	COM111	-9286.5	645.0		KEY_L	-9793.0	338.0
740	COM110	-9327.5	645.0		KEY_R	9793.0	338.0
741	COM109	-9368.5	645.0				
742	COM108	-9409.5	645.0				
743	COM107	-9450.5	645.0				
744	COM106	-9491.5	645.0				
745	COM105	-9532.5	645.0				
746	COM104	-9573.5	645.0				
747	COM103	-9614.5	645.0				
748	COM102	-9655.5	645.0				
749	COM101	-9696.5	645.0				
750	COM100	-9737.5	645.0				